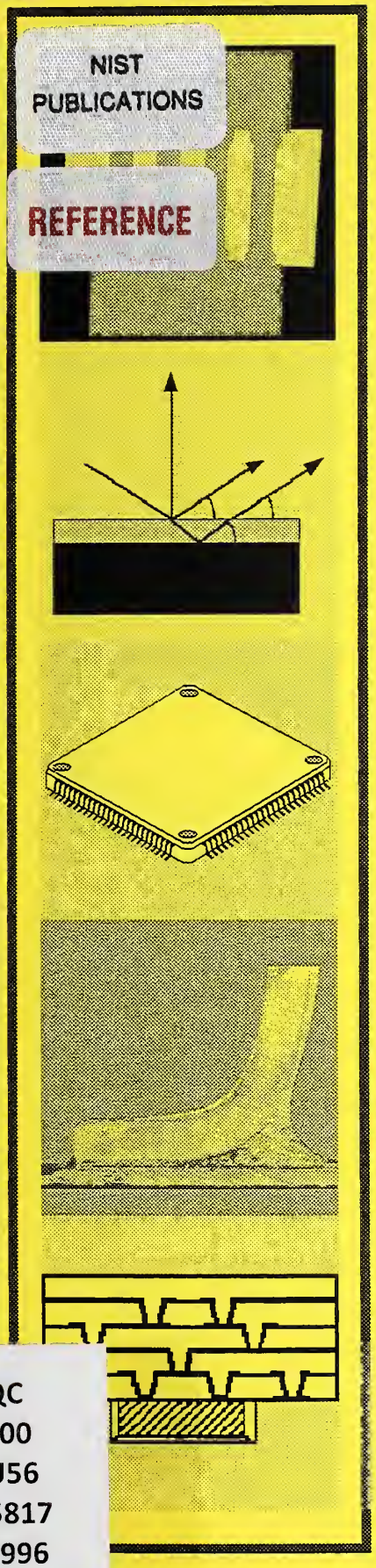
NAT'L INST OF STAND & TECH
A11107 160152

NISTIR 5817


NIST
PUBLICATIONS
REFERENCE

# ELECTRONICS PACKAGING, INTERCONNECTION AND ASSEMBLY AT NIST:

## GUIDE AND RESOURCES

Edited by

Michael A. Schen
National Institute of
Standards and Technology

U.S. Department of Commerce
Technology Administration

National Institute of Standards
and Technology

April 1996

NIST

QC
100
.U56
# 5817
1996

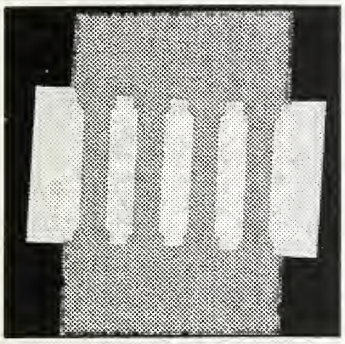
## On the Cover:

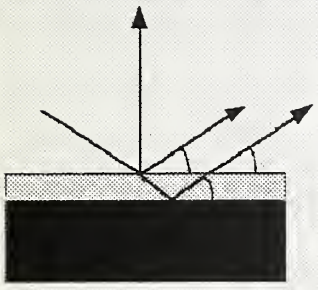
NIST scientists and engineers address a broad range of metrology issues involving materials and devices in electronics packaging, interconnection and assembly. The five schematics, from top to bottom, illustrate aspects of this work.

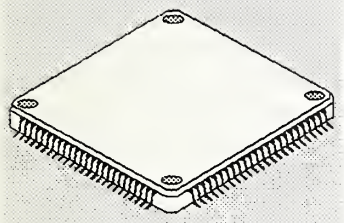
- Micrometer-scale dog bone arrays for evaluating *in situ* micromechanical properties of packaging and interconnection materials such as deposited metals and polymers.
- X-ray and neutron reflectivity studies on 10-200 nm thick polymer films to characterize the interfacial behavior and material properties of very thin films on substrates.
- Testing and modeling of the electrical and thermal characteristics of high speed, high performance semiconductor packages.
- Fundamental studies on solders, solderability testing, and solder joint design for peripheral and area array surface mount assembly.
- Thermomechanical and interfacial characterization of complex material assemblies found in emerging high density electronic interconnects.

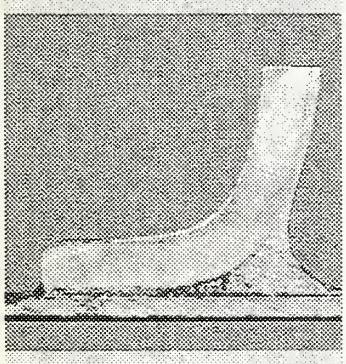
***Please note ...***

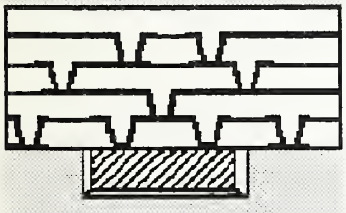
Commercial equipment, materials and organizations are identified in this report to adequately describe activities underway. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment, materials, or organizations identified are necessarily the best available for the purpose.











# ELECTRONICS PACKAGING, INTERCONNECTION AND ASSEMBLY AT NIST:

## GUIDE AND RESOURCES


Edited by

Michael A. Schen
National Institute of
Standards and Technology



U.S. Department of Commerce
Technology Administration

National Institute of Standards
and Technology

**NISTIR 5817**

April 1996



U.S. DEPARTMENT OF COMMERCE
Michael Kantor, Secretary

Technology Administration
Mary L. Good, Under Secretary for Technology

National Institute of Standards and Technology
Arati Prabhakar, Director

# *FOREWORD*

The U.S. microelectronics industry is confronted with technological changes at an unprecedented pace and urgency. This is partially due to increased consumer expectations, rapid product evolutions, and heightened international competition.

In response, the U.S. semiconductor industry and the module interconnection industry have developed technology roadmaps to identify technology roadblocks and enablers to insure continued competitiveness. A key element contained in these roadmaps is the packaging, interconnection and assembly of semiconductor components and the manufacture of electronic interconnects.

NIST has recently reinforced a series of laboratory-based efforts to further support the measurements and standards infrastructure of the U.S. commercial microelectronics industry in semiconductor packaging, electronic interconnection and assembly. In parallel, the Advanced Technology Program (ATP) is assisting the development in U.S. businesses of high-risk enabling technologies for new or improved products, manufacturing, processes, and services in electronic materials, semiconductor packaging, electronic interconnection, assembly and computer integrated manufacturing.

This publication, entitled *Electronics Packaging, Interconnection and Assembly at NIST: Guide and Resources,* presents a comprehensive inventory of NIST laboratory activities in this important technology arena. Intended to assist researchers and manufacturers, the *Guide* presents a concise snapshot of NIST research activities, the measurement capabilities and publications associated with each of these activities, and the names, telephone numbers and Internet addresses of people to contact for further information. In addition, the *Guide* presents a summary of ongoing ATP awards in the area.

# *TABLE OF CONTENTS*

FOREWORD ..... iii

TABLE OF CONTENTS ..... v

ACKNOWLEDGMENT ..... vii

NIST AT A GLANCE ..... 1

STRATEGIES AND ACTIVITIES ..... 3

LABORATORY PROJECTS ..... 5
Materials Metrology ..... 5
Semiconductor Packaging
Adhesion of Polymers: X-ray and Neutron Reflectivity Techniques ..... 5
Mechanics of Thin Interlayers: Viscoelastic and Fracture Behaviors ..... 6
Moisture Effects in Electronic Packaging Resins ..... 7
Polymer Cure and Performance ..... 8
Electronic Interconnection
Dielectric Measurements of Materials: DC to 1 GHz ..... 9
Dimensional Stability of Polymers ..... 10
Electromagnetic Properties of Materials ..... 11
Electron Beam Moiré ..... 12
Mechanical Properties of Thin Films ..... 13
Stress Voiding and Electromigration Damage in Thin Metal Films ..... 14
Assembly
Lead-free Solders ..... 15
Solder Interconnect Engineering ..... 16
Solder Jet Studies ..... 17
Solderability Measurements and Optimization ..... 18
Package-, Assembly-level Metrology ..... 19
Semiconductor Packaging
Metrology for Devices and Packages ..... 19
Electronic Interconnection
Electrical Characterization of Printed Wiring Board Interconnects ..... 20
Evaluation of Wire Bonding Technology ..... 21
High-Speed Electromagnetic Metrology ..... 22
Data Exchange ..... 23
Assembly
Automated Electronics Manufacturing ..... 23

ADVANCED TECHNOLOGY PROJECTS ..... 24
Materials
Low Dielectric Foams for Microelectronics Applications ..... 24
Ultra-low K Dielectric Materials for High Performance Interconnects ..... 25

Semiconductor Packaging
Flip Chip Monolithic Microwave Integrated Circuit Manufacturing ..... 26
Electronic Interconnection
Printed Wiring Board Interconnect Systems ..... 27
Scalable High-Density Electronics based on Multifilm Modules ..... 28
Assembly
A Product-Family-Based Framework for Computer Integrated Manufacturing ... 29
Solder Jet Technology Development ..... 30

APPENDIX I: ABBREVIATIONS ..... 31

APPENDIX II: COLLABORATIONS ..... 32

APPENDIX III: PUBLICATIONS ..... 33

INDEX ..... 42

# *ACKNOWLEDGMENT*

This NISTIR documents research activities that are being supported by NIST in a technology critical to the U.S. microelectronics industry. The *Guide* contains the contributions of over twenty-five different principal NIST researchers and managers who are working collaboratively with researchers and manufacturers from some 60 separate U.S. microelectronics and materials companies, consortia, trade associations, standards bodies, universities and other government agencies.

The editor is indebted to all the NIST staff who are identified in this *Guide* for their assistance in its production. This includes their contributions, suggestions and editorial review.

# *NIST AT A GLANCE*

The National Institute of Standards and Technology, or NIST, is a non-regulatory federal agency within the Commerce Department's Technology Administration. First established by the U.S. Congress in 1901 as the National Bureau of Standards, or NBS, the Institute was renamed and assigned new responsibilities in 1988.

The primary mission of NIST is to promote economic growth by working with industry to develop and apply technology, measurements, and standards. NIST carries out its mission through a portfolio of four major programs:

- **Laboratory Research and Services** - planned and conducted in cooperation with industry and focused on infrastructure technologies such as measurements, standards, evaluated data, and test methods;
- **Advanced Technology Program** - a rigorously competitive program that provides cost-shared grants to industry for development of high-risk pre-product, enabling technologies with significant commercial potential;
- **Manufacturing Extension Partnership** - a nationwide network of extension centers and experts co-funded by states and local governments that provides hands-on technical assistance to smaller manufacturers for adopting new technologies; and
- **Malcolm Baldrige National Quality Award** - a quality outreach program recognizing quality improvement by U.S. manufacturing and service companies.

**Budget:** $850 million (estimated post-rescission fiscal year 1995 from all sources)

**Staff:** About 2,900 scientists, engineers, technicians, and support personnel, plus some 1,300 visiting researchers each year

**Sites:** Gaithersburg, MD (headquarters), 234-hectare campus; Boulder, CO, 84-hectare campus.

## Laboratory Research and Services

NIST laboratory research and services provide the infrastructure technologies, such as measurements, standards, reference materials, evaluated data, and test methods, that U.S. industry needs to continually improve its products and services.

Planned and implemented in conjunction with U.S. industry through workshops, discussion forums, consortia, and extensive cooperative research efforts, NIST's research expertise includes electronics and electrical engineering, manufacturing engineering, chemical science and technology, physics, materials science and engineering, building and fire research, and information technology. NIST also provides industry with a range of technology services. These include Standard Reference Materials and Data, information on national and international standards, laboratory accreditation, and equipment calibration.

NIST's laboratory research efforts in electronics packaging, interconnection, and assembly draw upon experts in the areas of electronics and electrical engineering, and materials science and engineering.

## Advanced Technology Program

The Advanced Technology Program(ATP) invests directly in the nation's economic growth by working with industry to develop innovative pre-product technologies that have significant commercial potential but are too risky to be developed quickly without a partnership between industry and government.

Begun in 1990, the program provides cost-shared awards, through a rigorously competitive process, to both individual companies and industry-led joint ventures. It accelerates research progress on promising, but high-risk, enabling technologies that allow important improvements in products, processes, or services. ATP does not fund product development.

The ATP currently funds a number of projects in electronics packaging, interconnection and assembly through its general competitions.

## Manufacturing Extension Partnership

There are more than 370,000 U.S. manufacturers with fewer than 500 employees. These small and medium-sized companies account for about 95 percent of all U.S. manufacturing plants and about half of the nation's manufacturing capacity.

The Manufacturing Extension Partnership (MEP) is a nationwide network of affiliated manufacturing extension centers dedicated to helping smaller manufacturers improve their competitiveness by adopting modern technologies and production techniques. Each center is a partnership typically involving federal, state, and local governments; industry; educational institutions; and other sources of expertise, information, and funding support.

## National Quality Award

The Malcolm Baldrige National Quality Award has quickly become both the U.S. standard of quality achievement and a comprehensive guide to quality improvement. Congress established the award in 1987 to promote quality awareness, to recognize the quality achievements of U.S. companies, and to publicize successful quality strategies. In conjunction with the private sector, NIST developed and manages the award program.

A General Accounting Office report calls the award criteria, "the most widely accepted formal definition of what constitutes a total quality management company." About 1 million copies of the criteria have been distributed worldwide, and thousands of organizations are using the criteria as a quality improvement roadmap.

## Further Information

World Wide Web access
http://www.nist.gov/

General Inquiries
(301) 975-3058
inquiries@enh.nist.gov

Laboratory Programs
Electronics and Electrical Engineering
(301) 975- 4400
scace@nist.gov
http://www.eeel.nist.gov/

Materials Science and Engineering
(301) 975-6741
michael.schen@nist.gov
http://www.nist.gov/item/About_MSEL.html

Advanced Technology Program
(800) ATP-FUND
atp@micf.nist.gov
http://www.atp.nist.gov/

Manufacturing Extension Partnership
(301) 975-3593
mepinfo@micf.nist.gov
http://www.mep.nist.gov/

Malcolm Baldrige National Quality Award
(301) 975-2036
oqp@micf.nist.gov
http://www.nist.gov/nist/quality_program/

# *STRATEGIES AND ACTIVITIES*

**National Semiconductor Metrology Program**
Mr. Robert Scace, (301) 975- 4400, scace@nist.gov
**Advanced Materials Program**
Dr. Michael Schen, (301) 975-6741, michael.schen@nist.gov
**Advanced Technology Program**
Dr. Lura Powell, (301) 975-2627, lura.powell@nist.gov
**Publications:** Page 33.

NIST's activities in electronics packaging, interconnection and assembly are conducted within its laboratory research program and its Advanced Technology Program (ATP). This *Guide* presents a comprehensive description of laboratory research activities that directly support this portion of semiconductor and electronic interconnect manufacturing, and electronics assembly. In addition, the *Guide* presents a summary of ongoing ATP projects in the area. Readers are encouraged to contact the persons identified in the *Guide* to obtain further information or to discuss opportunities for joint research.

The NIST laboratory program is composed of two interrelated and coordinated efforts.

- National Semiconductor Metrology Program (NSMP)
- Advanced Materials Program (AMP)

Projects conducted under these two efforts draw upon experts in electronics and electrical engineering, and materials science and engineering. In addition a variety of projects are also underway within the Electronics and Electrical Engineering Laboratory as a part of that Laboratory's broader program to support the U.S. electronics industry. These projects provide package- and assembly-level measurement tools, reference standards and product data exchange standards needed by the semiconductor and electronic interconnects industries.

Performed in conjunction with industry and university partners, the projects conducted at NIST seek to reinforce six separate infrastructure and technology priorities described within the various national technology roadmaps [1,2] and planning documents derived from the roadmaps [3,4]. These six priorities include:

- Materials Metrology
- Package- and Assembly-level Metrology
- Modeling and Simulation
- Materials
- Data
- Standards

Technical input used to guide the planning and implementation of the projects described in this *Guide* is derived from industry-stated needs expressed in the roadmaps, as well as direct guidance obtained during workshops, meetings, collaborations or ongoing technical discussions.

Further information on any of these programs can be obtained by contacting the persons identified at the beginning of this section.

---

1 *National Technology Roadmap for Semiconductors*, Semiconductor Industry Association, 4300 Stevens Creek Blvd., Suite 271, San Jose, CA 95129, phone: (408) 246-2711.

2 *National Technology Roadmap for Electronic Interconnections*, Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062-6135, phone: (708) 509-9700.

3 Michael A. Schen, ed., *Metrology and Data for Microelectronic Packaging and Interconnection*, Results of a joint workshop, May 5-6, 1994, NISTIR 5520, November 1994.

4 *Electronics Manufacturing Technology Roadmaps and Options for Government Action*, National Electronics Manufacturing Framework Committee, Dec. 1994.

The following paragraphs provide a programmatic description of the laboratory-based and ATP efforts in electronics packaging.

## National Semiconductor Metrology Program

The National Semiconductor Metrology Program (NSMP) was established at NIST to develop and deliver useful **semiconductor metrology** to industrial clientele on a predictable schedule. The goals and objectives of the Program are directly linked to priorities contained within the National Technology Roadmap for Semiconductors. The Program is coordinated with allied efforts undertaken by SEMATECH and the Semiconductor Research Corporation (SRC).

NSMP presently supports research projects throughout NIST in semiconductor lithography, packaging, material and process characterization, and contamination control. In conjunction with scientists from the Materials Science and Engineering Laboratory, and the Electronics and Electrical Engineering Laboratories, NSMP supports activities aimed at developing useful and robust measurement tools and data for semiconductor devices and for the materials, processes, and structures used in today's - packaging schemes.

## Advanced Materials Program

The Advanced Materials Program (AMP) in electronics packaging and interconnection supports the manufacture of advanced microelectronic products by developing and delivering **measurement tools and data for materials and processes** used in **semiconductor packaging, electronic interconnection and component assembly**. The strategy used to implement this program is based upon four primary goals. They are:

- devise techniques and procedures for making *in-situ*, in-process and in-use measurements on materials and material structures having micrometer- and submicrometer-scale dimensions;
- record and quantify the divergence of material properties from their bulk values as dimensions are reduced and interfaces are approached;
- develop and disseminate standard measurements and data on materials in a form that can be used by industry; and
- develop fundamental understanding of materials used in contemporary packaging schemes.

AMP is strongly linked to the priorities contained in the national technology roadmaps for semiconductors and electronic interconnects and is coordinated with organizations which have a national role in technology development for the microelectronics industry. This includes the SRC, SEMATECH, the Interconnection Technology Research Institute (ITRI), the Semiconductor Industry Association (SIA), the Institute for Interconnecting and Packaging Electronic Circuits (IPC), and the National Center for Manufacturing Sciences (NCMS).

## Advanced Technology Program

The NIST ATP supports a number of industry-based high-risk technology development programs in electronics packaging, interconnection or assembly through its general competitions. Technology areas where grants have been awarded include electronic materials, semiconductor packaging, electronic interconnection, components assembly and computer integrated manufacturing.

# *LABORATORY PROJECTS*

## MATERIALS METROLOGY: *Semiconductor Packaging*

### Adhesion of Polymers: X-ray and Neutron Reflectivity Techniques

**Contact:** Wen-li Wu, (301) 975-6839, wen-li.wu@nist.gov
**Publications:** Page 33

Polymers are used pervasively in the packaging of microelectronic components for applications such as adhesives for die attach, interlayer dielectrics, molding compounds, encapsulants, and tape carriers in tape automated bonding. Since many of the failures experienced in polymeric electronic packages are initiated at polymer interfaces with materials such as silicon, silicon dioxide, copper, aluminum, and other polymers, it becomes important to understand the nature of these interfaces and the parameters that control adhesion.

In this project, the interfacial region is being studied by using X-ray and neutron reflectivity to measure the influence of interaction with the substrate on the physical properties of ultra-thin polymer films (50 to 1000Å). This work should lead to improved understanding of adhesion of polymers to dissimilar substrates such as those encountered in electronic packaging and advanced polymer composites.

These techniques allow for the determination of the density profiles of atomic composition in the interfacial region and for highly sensitive measurement of film thickness as a function of temperature from which glass transition temperature as well as coefficient of thermal expansion (CTE) can be determined. Analogous experiments in constant humidity environments also allow determination of material hygrothermal expansivity.

Development of methods for determining the adhesion strength between polymers and aforementioned substrates is also included in this project.

**Equipment:**

- NIST Research Reactor and neutron reflectometer for examining Angstrom thick films.
- X-ray reflectometer for thin film CTE and glass transition temperature measurements.
- Microbalance with optical attachments for determining the work of adhesion between solids.
- Contact angle goniometer with controlled environment chamber (Vacuum Atmospheres, Inc.).

# MATERIALS METROLOGY: *Semiconductor Packaging*

## Mechanics of Thin Interlayers: Viscoelastic and Fracture Behaviors

Contact: Greg McKenna, (301) 975-6752, gregory.mckenna@nist.gov
Martin Chiang, (301) 975-5186, martin.chiang@nist.gov

**Publications:** Page 34

A major problem in developing design criteria for electronic packages and interconnects is the inability to measure and model material properties of relevance in extremely thin polymeric films. This is especially true for the micromechanical and fracture characteristics. Hence a methodology to study and predict the viscoelastic and viscoplastic response of thin layers is important to the packaging industry and their future products.

This NIST project is addressing these problems by developing methods to measure the thin film response of polymers in shearing deformations at thickness ranges from 2 to 25 $\mu$m and by developing finite element models with appropriate failure criteria for comparison with model thin film adhesive systems. These dimensions are typical of polymer thin film applications in semiconductor packaging or high density interconnect substrates. In this project, napkin ring geometry samples with thicknesses ranging from 2-25 $\mu$m are being used in different load and temperature conditions as the starting point for development of a method to determine the large deformation response of thin polymer layers or films. The information gained from these tests is being incorporated into elastic-plastic finite element models of thin interlayers. Evidence suggests that modeling of the polymers used in packaging applications need to incorporate nonlinear and time-dependent constitutive behaviors to fully account for the observed fracture behavior.

It is anticipated this work will result in mechanical testing techniques that can be used to characterize the mechanical response of polymers in constrained or very small geometries. This will allow thin film material response data to be compared with data from macroscopic samples. Finite element models can then be used to determine how important the property differences are for model fracture toughness experiments and for typical electronic packaging applications.

**Equipment:**

- Servo-hydraulic mechanical testing equipment (Instron, MTS).
- Video microscope and recording system.
- ABAQUS Finite element analysis package for workstation.
- Computer workstation (Silicon Graphics Inc.).
- Stereo microscopy.

# MATERIALS METROLOGY: *Semiconductor Packaging*

## Moisture Effects in Electronic Packaging Resins

**Contact:** Greg McKenna, (301) 975-6752, gregory.mckenna@nist.gov
David VanderHart, (301) 975-6754, david.vanderhart@nist.gov

**Publications:** Page 34
**Related Work:** Page 8

The intrusion of moisture into the resins used in electronic packaging is a major problem in manufacturing and the subsequent performance of electronic devices. For example, the presence of moisture and its distribution in the resin have potentially deleterious effects during soldering of these devices onto circuit boards owing to problems such as the 'popcorn' effect, i.e. the splitting open of the resin package. Long term performance of devices can be compromised when moisture attacks the filler/resin interface due to a degradation of mechanical properties. Finally, water-induced degradation of the interfaces between the package and the device may lead to corrosion-induced failure. It is, therefore, highly desirable to have a fundamental understanding of the nature and distribution of water in electronic packaging materials. This knowledge will also be helpful in establishing more realistic models for the development of hygrothermal stresses in a typical chip package.

This project has the goal of developing a fundamental understanding of moisture distribution and the kinetics of moisture uptake in electronic packaging materials and chip encapsulant resins in particular. In these materials moisture can reside in the resin; at the resin/filler, resin/metal and resin/silicon interface; in voids which result from entrained air; and, in the case of porous fillers with interior surface area, within the filler itself. NIST is using solid state nuclear magnetic resonance (NMR) spectrometry to study the presence and distribution of water in both the filled and unfilled encapsulant resins, and as appropriate in the filler itself.

**Equipment:**

- 200 MHz solid-state proton NMR spectrometer with fast recovery times, magic-angle sample spinning, and capabilities for multiple-pulse irradiation.

# MATERIALS METROLOGY: *Semiconductor Packaging*

## Polymer Cure and Performance

Contact: G. Thomas Davis, (301)975-6725, george.davis@nist.gov
Publications: Page 34
Related Work: Page 7

Polymers are essential components of modern electronics. Whether used as adhesives, dielectric layers, encapsulants or electrical interconnects, the polymers used in electronic packaging are typically applied as precursors which are changed into their final forms during manufacture. This NIST project has the primary objective of providing resin suppliers, chip manufacturers and instrument makers with reliable data and test methods for:

- monitoring the cure of industrially important resins during manufacture;
- following and characterizing the moisture uptake of polymers during storage and service; and
- monitoring the effects of cure and moisture uptake on residual stress and thermal conductivity.

Infrared-based photoacoustic spectroscopy has been studied as a means of monitoring the chemical and physical changes that take place during the cure of polyimides. The technique has been shown to provide information on the nature of a polymer layer while adhered to an opaque substrate. From the cumulative infrared absorption spectra as a function of film depth, a spectral "finger-print" of the film allows quantitative film-to-film comparisons.

To gain insights into the nature and effects of moisture in packaging resins, NIST is conducting studies on encapsulation resins. Popcorning is a major problem in the assembly of large, thin semiconductor packages. To further understand popcorning, NIST is using near infrared spectroscopy to determine the quantity and physical state of absorbed moisture, and is using wafer-bending equipment and a thermal pulse technique to examine the effects of moisture on properties such as residual stress and thermal conductivity.

**Equipment:**

- Photoacoustic attachment (MTEC 200) for Fourier transform infra-red (FTIR) spectrometer.
- Thin film stress measurement system (Tenco FLX2320).
- NIST-built thermal pulse apparatus for charge/polarization distribution and thermal conductivity measurements.

# MATERIALS METROLOGY: *Electronic Interconnection*

## Dielectric Measurements of Materials: DC to 1 GHz

Contact: Fred Mopsik, (301) 975-6747, frederick.mopsik@nist.gov
Publications: Page 34
Related Work: Page 11, 22

Insulation used in electronics applications must meet high performance standards over a very wide range in frequency. As the operating frequency of ICs increase and the spacing between conductors decrease, the insulation can become the limiting factor in the performance of systems. Some of the most desirable materials are often available only as thin films, creating additional measurement problems at higher frequencies. Current practice, even at 1 MHz, has sufficient uncertainty to create problems for the semiconductor industry. While low frequency techniques developed in this laboratory can cover the range from direct current (DC) to 10 kHz, higher frequencies require different methodologies.

To provide more reliable measurement methods, this project is working to develop techniques to accurately measure the dielectric performance of thin film polymeric insulators used in electronics packaging and interconnection applications. These high frequency methods will then be added to existing low-frequency methods to extend the frequency range to 1 GHz for low loss materials. The results of this project will lead to the development of measurement standards usable by the electronics industry to generate reliable design data on insulation systems including polymer thin films.

Four-terminal precision inductance, capacitance, resistance (LCR) meters covering the frequency range from 100 Hz to 30 MHz have been added to existing time-domain instrumentation and a 1 MHz to 1 GHz impedance analyzer. Measurement uncertainties and calibrations for the instruments have been completed and a sample holder has been designed for use in both three- and four-terminal configurations so that only a single sample is needed for measurements from DC to 30 MHz. Initial data on polyimide films have shown the limits of the commercial instrumentation and indicate unreliable loss values toward the high frequency portion of a given instrument's frequency range. Results also show that reliable dielectric constant and loss data, with a relative error of better than 0.1% just above 10 KHz, increasing to 1% at 1 GHz, on thin film materials should be possible.

**Equipment:**

- NIST-built time domain spectrometer from 1 MHz-10 kHz.
- RF/microwave instrumentation (includes HP4285A precision LCR meter from 75 kHz to 30 MHz; HP4191A impedance analyzer from 1 MHz to 1 GHz; Andeen-Hagerling 1 kHz ultra precision capacitance bridge).

# MATERIALS METROLOGY: *Electronic Interconnection*

## Dimensional Stability of Polymers

Contact: Michael A. Schen, (301) 975-6741, michael.schen@nist.gov
Publications: Page 35

Today's microelectronics products rely heavily on the use of polymeric materials; whether to package and protect the integrated circuit or to manufacture printed wiring boards and assemblies. A key parameter for the design and reliability of polymer containing products is the out-of-plane coefficient of thermal expansion (CTE). Consequently, the ability to routinely measure and produce high quality data on polymer z-CTE is critical for future high density packaging and interconnection schemes.

This NIST project is part of a broad-based NIST approach to improve the capabilities available to industry to measure and understand the dimensional stability of polymeric materials typically used in electronics packaging and interconnection schemes. Focusing specifically on z-CTE, this research utilizes a two pronged strategy that first seeks to improve existing metrology commonly used in industry to measure z-CTE and second to develop manufacturing- and research-based tools with enhanced sensitivity and accuracy to understand the behavior of polymer thin films.

The project is focused on two activities. The first is to improve the methodologies and test standards presently employed in industry using a commercially available thermal mechanical analyzer (TMA). In conjunction with industry and academia, NIST is developing an improved TMA testing methodology that utilizes silicon single crystal as a working standard against which polymer measurements are evaluated and is evaluating the uncertainties associated with the measurement. Second, NIST has successfully developed and demonstrated a dimensionally stable, nearly constant electrode area capacitance cell that can accurately measure the thermal expansion of silicon single crystal over a broad temperature range. Viewed to be a much superior technique for measuring z-axis CTE, the technique is being applied to the characterization of thin polymer films used in microelectronics manufacturing.

**Equipment:**

- High precision capacitance cell for z-CTE measurement.
- Environmental temperature, humidity chamber (under construction).
- Ultra-precision capacitance bridge (Andeen-Hagerling, 1 kHz).

# MATERIALS METROLOGY: *Electronic Interconnection*

## Electromagnetic Properties of Materials

**Contact:** Claude Weil, 303-497-5305, claude.weil@nist.gov
**Publications:** Page 35
**Related Work:** Page 9, 22, 20

Dielectric and magnetic materials have wide application throughout the electronics, microwave, communication and aerospace industries. Their applications in microelectronics include printed circuit boards, substrates, interlevel "low-k" dielectrics, dielectric and ferrite thin-films, hybrid electronic components, etc. NIST works closely to support the microelectronics and wireless industries in a number of critical areas: a) evaluating and improving measurement methods used to characterize the complex permittivity and permeability of many dielectric and magnetic materials over the RF/microwave spectral range of 300 kHz to 75 GHz, b) providing well-characterized standard reference materials, c) providing measurement services to customers, and d) organizing measurement intercomparisons.

This project is involved in two research tasks that have specific application to microelectronics and wireless. First it seeks to support the ATP-funded industry consortium on printed wiring board (PWB) interconnect systems by developing improved methods for characterizing the dielectric properties of PWBs at frequencies up to approximately 6 GHz. Much of this effort has centered on low-frequency capacitor techniques, re-entrant coaxial cavities and the split-cylinder ("Kent") cavity, both air and dielectrically filled. The second is a collaborative effort with the High Speed Microelectronics Metrology Project to perform in-situ measurements of the dielectric properties of substrates and dielectric thin films used in digital and monolithic microwave integrated circuits (MMIC). This effort has been expanded in FY 96 to include SEMATECH, who will fabricate IC test structures.

**Equipment:**

- RF/microwave instrumentation (includes HP-8510B automatic network analyzer from 50 MHz to 18 GHz, HP-8753C ANA from 300 kHz to 6 GHz, HP-8751A ANA from 5 Hz to 500 MHz, HP-4291A RF Impedance/Materials Analyzer from 1 to 1800 MHz, HP-4284A Precision LCR Meter from 20 Hz - 1 MHz).
- Sampling components (includes 7-, 14- and 77-mm diameter coaxial air line and WR-90; WR-284 waveguide components; 3.5 and 14 mm diameter open-ended coaxial probes; cavity resonator fixtures for operation from 150 MHz to 75 GHz).
- Cryostat system for low temperature measurements, from 4 - 120°K .
- High field strength DC electromagnet.

# MATERIALS METROLOGY: *Electronic Interconnection*

## Electron Beam Moiré

Contact: David Read, (303) 497-3853, david.read@nist.gov
Publications: Page 35

Experimental mechanics measurements have been used in conjunction with modeling and simulation to optimize many critical or high-performance macro scale structures such as nuclear pressure vessels and aircraft. Accurate calculation of stresses allows quantitative failure prediction and analysis, where the specific stress levels responsible for a failure can be determined, and can be compared to the critical material parameter for that specific failure mode. The purpose of this project is to enable this same level of sophisticated mechanical engineering for advanced electronic interconnect structures. Quantitative experimental measurements of displacements on the microscale are needed to verify that modeling and simulation results are accurate and to guide the analysis. Experimental mechanics observations allow the workings of the failure modes to be examined before and during failure.

Optical moiré techniques including geometrical moiré and moiré interferometry have advanced to a high level of sophistication. Use of electron beam moiré takes advantage of the greater magnification and depth of field of the scanning electron microscope to extend moiré techniques further into the microscale. The technique requires the writing of a line- or cross-grating on the specimen surface. When the spacing of the raster scans of the SEM nearly matches the grating pitch, a geometrical interference occurs, and moiré fringes are produced in the SEM image. The density of moiré fringes is proportional to the strain relative to the reference state.

We have verified this technique on a classical fiber-matrix composite using mechanical loading. For electronic interconnect structures the stresses are thermomechanical, so these are not loaded mechanically, but instead are heated or cooled *in situ* in the SEM. We use this procedure to examine the thermomechanical behavior of plated-through-holes in printed wiring boards and of a copper-polymer high density interconnect structure. We are currently studying mechanical behavior of interfaces in conductive adhesives, both isotropic and anisotropic, and strains at the solder ball interfaces in ball grid arrays.

Currently, 0.1-$\mu$m-pitch line gratings over a 50-$\mu$m field of view can be used in some materials. Coarser gratings are used on highly heterogenous interconnect structures. A heating-cooling stage in the scanning electron microscope (SEM) allows examination of thermomechanical strains at temperatures from -50 to +150 °C. Analysis of the digitally-acquired SEM images allows NIST to quantify strains within cross-sectioned devices and compare them to predictions from finite element modeling.

Comparison of experimental results with modeling and simulation is much more useful than experimental results alone. We look to collaborators in academia and industry in order to undertake projects that include both experimental and numerical components.

**Equipment:**

- Scanning electron microscope, including special accessories for electron beam lithography.
- Mechanical and thermal testing stages for the SEM.
- Digital image acquisition and analysis software for extracting displacements and strains.

# MATERIALS METROLOGY: *Electronic Interconnection*

## Mechanical Properties of Thin Films

Contact: David Read, (303) 497-3853, david.read@nist.gov
Publications: Page 36

The micromechanical properties of thin metal and polymer films are fundamental to the manufacturability and reliability of advanced integrated circuits and interconnect systems. The thin metal layers found in advanced interconnection structures are fabricated using special techniques such as physical vapor deposition and eletrodeposition. Hence their microstructures and their mechanical properties are usually quite different from those of the bulk material with the same chemical composition. Consequently, test procedures optimized for bulk materials often cannot be applied to materials found in packaging and interconnect structures. NIST is working with the microelectronics and materials industries to apply micromechanics to their problems and to provide useful data on industrially important materials and structures. This project has two primary goals:

- develop *in-situ* measurement techniques for micromechanical properties; and
- develop accurate material mechanical property information.

NIST has developed a method that accurately measures the mechanical properties of thin films and is using it to study the mechanical properties of suspended films of aluminum and copper. Specimens are produced using micro-photolithography steps similar to those used in the fabrication of electronic interconnect structures. A specimen film is deposited by electron beam evaporation, sputtering, or electrodeposition on a pre-patterned silicon substrate. The film is patterned to form narrow strips similar in shape to standard tensile coupons used for sheet metal, except much smaller. The silicon is removed from underneath the gage sections by etching, leaving the tensile specimen freely suspended across a silicon frame. Tens of such specimens can be produced on a single silicon wafer. The gage section of the tensile specimen is 200 $\mu$m wide by 700 $\mu$m long. Specimens from 0.25 to 2.5 $\mu$m thick have been tested. One of the goals of the project is to reduce these dimensions to sizes closer to those used in interconnect layers on modern integrated circuits. These have similar thicknesses, but widths less than 1 $\mu$m.

A custom-made microtensile apparatus is used to test these specimens. The tester is rigid enough to allow the silicon frame to be severed without damaging the specimen. Piezoelectric stacks provide tensile displacements controllable to a few tens of nanometers. Closed loop control allows ramp or sinusoidal load or displacement functions to be applied. The tester fits into a microscope, so the specimen can be observed during the test.

Results to date indicate that the yield and ultimate strengths of pure copper and aluminum thin films are considerably higher than these same materials in bulk form. This behavior can be explained by the very small grain sizes of the thin films. The films tested to date have a much lower elongation to failure than the handbook values for bulk materials. These elongation values are also less than elongations reported for thicker specimens of materials with comparable grain sizes. Tensile tests within the transmission electron microscope are being used to study this behavior. It is believed that in the thin films dislocations are more likely to escape from the surface and to accumulate at grain boundaries, and are less likely to travel long distances, compared to bulk materials.

The closed-loop, piezoelectric-driven tester also lends itself conveniently to fatigue studies. For example, during a recent evaluation of the tension-tension fatigue resistance of copper thin films, several specimens survived past 10,000 fatigue cycles, and one lasted beyond 100,000.

**Equipment:**

- Thin film fab for specimen preparation.
- Microtensile test apparatus.

# MATERIALS METROLOGY: *Electronic Interconnection*

## Stress Voiding and Electromigration Damage in Thin Metal Films

**Contact:** Robert Keller, (303) 497-7651, bob.keller@nist.gov
**Publications:** Page 36
**Related Work:** Harry Schafft, (301) 975-2234, harry.schafft@nist.gov

Microelectronics technology has evolved to the point where metallizations have sub-micron dimensions. As a result, failures due to localized phenomena such as stress voiding and electromigration are an increasing reliability concern. Stress voiding develops during microelectronics processing and is accelerated at higher temperatures. Subsequent electrical current stressing can then lead to additional void formation and growth.

Most voidage and electromigration investigations employ accelerated tests to approximate in-service conditions and address issues such as median time to failure and void content. More recently, correlations between void location and metallization geometry have been made. Interconnect research examining microstructural variables is in its earliest stages, and localized microstructural information is still lacking. In addition, *in situ* microstructural investigations have taken place to refine or verify specific model predictions related to the role of localized diffusion and local stresses and strains in interconnect failure.

This project seeks to assess the role of crystallography in the development of local stress and strain within interconnect lines subjected to thermal stressing and high current density testing. Issues such as grain boundary geometry and orientation are considered. The project uses a backscatter Kikuchi diffraction (BKD) technique in the scanning electron microscope to determine localized crystallographic orientations and lattice parameters, both of which are direct reflections of the stress and strain states of the metal films. The technique extracts information from small regions of approximate diameter 0.3 to 0.5 $\mu$m (and depths 0.05 to 0.1 $\mu$m), using de-passivated metal films which remain on bulk substrates.

**Equipment:**

- High spatial resolution BKD camera system for scanning electron microscope (under construction).
- 30 kV scanning electron microscope equipped with electron detector showing high sensitivity to both crystallographic and topographic contrast.
- 200 kV transmission electron microscope equipped with a scanning unit for high spatial resolution chemical and diffraction analyses.

# MATERIALS METROLOGY: *Assembly*

## Lead-free Solders

**Contact:** Carol Handwerker, (301) 975-6158, carol.handwerker@nist.gov
**Publications:** Page 37
**Related Work:** Page 18

Because of industrial and governmental concern about possible hazards from lead contamination in the environment, identification of lead-free solders has become a high industrial priority and technological challenge. The importance of this challenge was recognized by the high priority given to the identification of alternatives to lead-containing solders in both the semiconductor and electronic interconnects technology roadmaps.

To help accelerate the development of lead-free alternatives, the National Center for Manufacturing Sciences (NCMS) has established a lead-free solders consortium. The objective of this consortium is to develop environmentally safe alternatives for the lead-based solder alloys currently used for electronic interconnections. These alternatives must meet stringent manufacturing, performance and environmental requirements set by industry. NIST is assisting this industry-based development program through the following tasks:

- determination of critical tests for alloy development;
- calculation and experimental determination of multi-component phase diagrams critical for evaluating candidate alloys;
- identification of new alloys for evaluation based on phase diagrams;
- fabrication of candidate alloys for testing by consortium members; and
- modeling of solder wettability and solderability.

By providing this support, NIST is helping to significantly reduce the number of candidate systems undergoing full industry evaluation within the consortium.

**Equipment:**

- Alloy melting, casting, rolling, and atomization facilities
- Differential thermal analysis.
- Metallographic analysis including optical and electron microscopy, mechanical properties testing laboratory.

# MATERIALS METROLOGY: *Assembly*

## Solder Interconnect Engineering

**Contact:** Carol Handwerker, (301) 975-6158, carol.handwerker@nist.gov
**World Wide Web:** http://www.ctcms.nist.gov/programs
**Related Work:** Page 18

As microelectronic circuits go to finer pitches and higher I/O counts, open circuits and solder "bridges", in which short circuits form between neighboring interconnects during soldering operations, have become a major problem. Furthermore, the use of surface mount technology and area array interconnects has increased the mechanical and thermal demands on solder joints. In order for solder or other materials, such as conductive epoxies, to satisfy the increasingly high demands placed on them, design, manufacturing, and reliability must become integrated.

This NIST project is working with numerous industry and university partners to develop a software tool that integrates component interconnect design, solder joint manufacturing, thermal management, and thermo-mechanical reliability. The project is comparing the applicability of various algorithms to predict solder joint geometries for standard geometries of special interest to industry. These algorithms will be used to predict the sensitivity of the design to variables in materials and manufacturing processes.

**Equipment:**

- Computer facility for the development of software tools (consists of workstations and personal computers).

# MATERIALS METROLOGY: *Assembly*

## Solder Jet Studies

**Contact:** Frank Gayle, (301) 975-6161, frank.gayle@nist.gov
**Related Work:** Page 18

The printing of solder patterns onto chips or circuit boards using ink jet printer technology is a novel means to avoid cumbersome screening techniques and environmentally unfriendly electroplating methods. In addition, "solder jet" technology is flexible and capable of very fine pitch, <100 $\mu$m, between solder deposits. These capabilities are needed for future fine interconnect pitch semiconductor packages.

This NIST project is working with equipment manufacturers and a U.S. solder jet consortium to bring solder jetting technology closer to commercial reality. In this project, NIST is focusing on two primary issues:

- materials compatibility between the liquid solder and the jetting apparatus; and
- reactions between the jetted solder and the various substrate materials used in microelectronic interconnects.

Encompassed within the scope of the project is the determination of requirements for reliable solder jet operation and joint performance, and the characterization of solder jet deposits with a range of deposition conditions and substrates.

**Equipment:**

- Optical metallography.
- Scanning electron microscopy.
- Windowless energy dispersive spectroscopy.
- Electrochemical testing and characterization.
- Alloy melting, casting, rolling, and atomization facilities.
- Differential thermal analysis.
- Metallographic analysis including optical and electron microscopy.
- Mechanical properties testing laboratory.

# MATERIALS METROLOGY: *Assembly*

## Solderability Measurements and Optimization

Contact: John Manning, (301) 975-6157, manning@nist.gov
Publications: Page 37
Related Work: Page 15, 16

As microelectronic devices become smaller and smaller, the decreasing size of the solder joints places increasing demands on the soldering process itself. Good first-pass solderability and establishment of tests to predict solderability before committing components to the production line are therefore important industrial goals. In this project, NIST is working to develop solderability measurement techniques that help reach the target dimensions for fine pitch and area array interconnections identified in the technology roadmaps for semiconductors and electronic interconnects. The project is engaged in three primary efforts:

- improved tests for solderability;
- effects of intermetallic formation on solderability; and
- statistical analysis of new steam aging test as an accelerated test for solderability.

In the area of solderability testing, NIST scientists are examining the physical basis for the wetting balance test, a commonly used test for solderability, and reasons for discrepancies between this test and actual component soldering. In addition, alternative solderability tests based on electrochemical techniques are being examined that provide more reproducible measurements of initial solderability and the loss that can occur during storage. The effects of intermetallics on solderability also are being investigated.

To optimize solder joint design, NIST is evaluating solder joint manufacturability and reliability by evaluating wettability using the wetting-balance test and solderability degradation through accelerated aging tests. These and related efforts have led to the development of a method for extracting time-temperature-solder contact angle data from wetting balance and area-of-spread tests. Using this, data for groups of substrate/flux/solder combinations have been generated to assist the design of soldering processes and to evaluate the sensitivity of solder alloys to changes in flux. This work is linked to new steam aging tests being evaluated for solderability testing.

**Equipment:**
- Wetting balance.
- Electrochemical measurement systems.

# PACKAGE-, ASSEMBLY-LEVEL METROLOGY: *Semiconductor Packaging*

## Metrology for Devices and Packages

**Contact:** David Blackburn, (301)975-2068, david.blackburn@nist.gov
**Publications:** Page 38
**Related Work:** Page 22

NIST has made technical and leadership contributions to all of the significant microelectronic device and package thermal standards now in use in the U.S. In this project, these efforts have been expanded to include the development of improved methods for characterizing and specifying the thermal and electrical properties of microelectronic packages and model validation.

In the thermal arena, NIST has developed a model for the steady-state surface temperature of multilayer structures with an arbitrary number of layers. This new code is particularly appropriate for studying thermal management of new devices and packages. Motivation for this work comes from dissatisfaction with existing thermal resistance specifications that do not take the detailed device environment, such as use of a heat sink, forced or natural convection, high or low thermal conductivity circuit board, etc. into account. NIST originally developed the concept of "compact thermal models" and has subsequently developed a formalism for implementing this concept in SABER™, a commercial system simulator by Analogy, Inc. Comprehensive thermal characterization procedures and facilities at NIST are being used in support of this new concept.

In the electrical arena, NIST is concentrating on the metrology required to extract the package parasitics that are so important to circuit performance. Time domain reflectometry is used as a complement to more traditional frequency domain measurements. The ultimate objective of this effort is to provide metrology and validation support for comprehensive models that merge package electrical and thermal characteristics with those already existing for individual chips.

**Equipment:**

- Thermal analysis lab (includes scanning IR microradiometer for surface temperature maps).
- Interconnect parameter analysis system for electrical interconnect analysis.
- Sun Sparc20 workstations.
- 3D solid (ANSYS, PC3D) and computational fluid dynamics (FLOTRAN, U. Maryland Code) modeling and simulation.
- 3D electrical interconnect modeling (Technology Modeling Associates 'Raphael').

# PACKAGE-, ASSEMBLY-LEVEL METROLOGY: *Electronic Interconnection*

## Electrical Characterization of Printed Wiring Board Interconnects

Contact: Nicholas Paulter, (301) 975-2405, nicholas.paulter@nist.gov
Publications: Page 38
Related Work: Page 22

Optimization of the electrical performance of chip interconnects is becoming increasingly important as multichip modules see greater use and as the gap narrows between circuit densities of the printed wiring board, or high density substrate, and that of the semiconductor package. Consequently, readily available and easy to apply methods appropriate to the task of measuring the high frequency performance of these interconnects are needed.

This project has the primary focus of using pulse-measurement technology and appropriate analysis to extract electrical information, in the form of either time- or frequency-domain parameters, pertaining to the performance of printed wiring board interconnects. The time-domain measurements yield information on characteristics such as pulse aberration, delay, attenuation, impulse response, and cross-talk. Through a Fourier transform analysis, the time-domain information provides frequency-domain characteristics such as dispersion, loss, transfer function, and scattering parameters. This approach can be used to study material characteristics, electro-migration, and interconnect performance within the package.

Present activities have focused on the development of a "factory-floor" measurement technique for determining the dielectric constant of printed wiring board dielectrics and on the assessment of measurement uncertainty and stability. The work is being expanded to include extraction of dielectric loss and identification of temperature dependencies.

**Equipment:**

- High-speed electrical pulse measurement from DC to 20 GHz: consists of 20 GHz and 50 GHz oscilloscopes; high-accuracy 2 GHz sampling system; high-bandwidth pulse generators; and high-frequency synthesizers.
- PWB CAD and simulation (consists of schematic capture and routing program [PADS-Perform(TM) by PADS] and a Spice-based circuit simulator [Analog Workbench by Cadence]).

# PACKAGE-, ASSEMBLY-LEVEL METROLOGY: *Electronic Interconnection*

## Evaluation of Wire Bonding Technology

**Contact:** George Harman, (301) 975-2097, george.harman@nist.gov
**Publications:** Page 38

Wire Bonding is the most pervasive method for interconnecting microelectronics chips to their packages. Currently there are about $4x10^{12}$ of such interconnections made per year. The nearest competing interconnection technology is only about 2-4% of this value.

To assist industry in their use of wire bonding technology, NIST is working with other laboratories in evaluating bonding methods to soft substrates and multichip modules, as well as investigating methods to enhance the application of wire bonding in fine pitch bonding. In addition, the second edition of the book *Reliability and Yield Problems of Wire Bonding in Microelectronics* by G.G. Harman is in preparation and scheduled to be published by McGraw Hill in 1996.

# PACKAGE-, ASSEMBLY-LEVEL METROLOGY: *Electronic Interconnection*

## High-Speed Electromagnetic Metrology

**Contact:** Roger Marks, (303) 497-3037, roger.marks@nist.gov
Dylan Williams, (303) 497-3138, dylan.williams@nist.gov

**Publications:** Page 39
**Related Work:** Page 9, 11, 20

For many years, the telecommunications industry has demanded advances in metrology for radio frequency and microwave electronics. The explosion in the sophistication and popularity of wireless communication products has reinforced this trend. In the meantime, faster processing speeds and more stringent signal integrity demands have presented the digital packaging industry with similar measurement requirements.

This project is focused on developing and disseminating electrical measurement methods for the accurate electrical characterization of interconnection and packaging structures for high-speed microelectronics circuits and of radio frequency (RF) and microwave integrated circuits. Specific activities include:

- developing improved, accurate calibration and measurement procedures for use with network analyzers and on-wafer probe stations;
- modifying time domain instruments for use in frequency-domain package characterization;
- conducting measurements of scattering parameters, impedances, and transmission line parameters on high speed interconnections;
- developing accurate electrical characterization methods for flip-chip monolithic microwave integrated circuits (MMIC) circuit elements, including passive components, solder joints, and bridges;
- developing procedures to characterize crosstalk;
- developing techniques to characterize thin-film dielectrics using on-wafer measurements;
- disseminating methods by distribution of measurement software;
- fabricating test structures for use in experiments and as calibration standards; and
- initiating and leading industrial standardization efforts.

**Equipment:**

- 40 GHz vector network analyzer.
- Time-domain network analyzer system.
- On-wafer probe stations.
- Clean room facilities for processing passive GaAs and Si wafers.
- Metallization for coplanar waveguide and microstrip structures.
- Reactive ion etching for via formation.
- Microstrip backside processing, including wafer lapping and polishing.

# DATA EXCHANGE: *Assembly*

## Automated Electronics Manufacturing

Contact: James St.Pierre, (301) 975-4124, james.st.pierre@nist.gov
Publications: Page 41
World Wide Web: http://www.eeel.nist.gov/811/eitg/aemp.html

Product standards and specifications are key enablers in the design, manufacture, documentation, procurement, and support of modern electronic products. Traditional formats for capturing designs and manufacturing information are rapidly being replaced by digital formats which must be correct, complete, unambiguous, and efficient. To realize wide-spread use of interchangeable electronic product data, the development of adequate information models and standards that unambiguously express product designs and that "harmonize" existing data transfer standards are required.

This NIST program assists industry in the technical development of neutral product data exchange specifications and automation frameworks for the electronics industry. This is accomplished by providing an impartial forum in the form of a testbed to resolve conflicts among competing and conflicting standardization efforts within the electronics industry, including those affecting manufacturers of packaged semiconductor devices and printed wiring boards, and those who need these parts for the design, manufacture, and repair of electronic systems.

Problems being addressed in this effort include lack of interoperability between tools; information loss, corruption or distortion during transfer from system to system; and bypassing traditional distribution of component and design information to alleviate bottlenecks in the design process.

Current activities underway in the program include the following four tasks.

- **Initial Graphics Exchange Specification (IGES) of Layered Electrical Products (LEP) Application Protocol (AP).** NIST is very involved in the technical development and evaluation of the IGES LEP AP. The AP is intended to represent design information for layered electrical products such as printed circuit boards and multi-chip modules (MCM's). This capability will enhance the ability of designers to exchange engineering design files via the Internet.

- **Computer Integrated Manufacturing Framework (CIMF).** NIST is assisting SEMATECH in the technical and business development of a CIMF. When instituted within the semiconductor industry, CIMF will reduce integration costs for new fabrication facilities and shorten lead times for getting new products to market.

- **Microwave and Millimeter-wave Advanced Computational Environment (MMACE).** NIST is providing technical assistance to the Department of Defense MMACE project by helping in the selection of the most appropriate protocol technologies for their application and by contributing to the development of software prototypes and educational tools. MMACE is a Tri-Service effort to develop a comprehensive computational design environment for microwave power tubes that uses Internet ftp, telnet, X Windows, and WWW protocols to link collaborators in diverse locations.

- **Standard for the Exchange of Product Model Data (STEP) Application Protocol 210 (AP210).** NIST has been very active in the development and evaluation of STEP AP210. The intent of AP210 is to represent printed circuit assemblies (PCAs) and printed circuit boards (PCBs) in a means consistent with other STEP AP's, and allow PCB and PCA design data to be incorporated into the life cycle design flow of large systems consisting of electrical and mechanical components.

**Equipment:**

- Computer testbed for testing electronic product data exchange standards, engineering frameworks, and conformance testing of related standards.

# *ADVANCED TECHNOLOGY PROJECTS*

## *Materials*

### Low Dielectric Foams for Microelectronics Applications

**Participants:** IBM Corp. San Jose, CA
**Industry Contact:** Michael Ross, (408) 927-1283
**ATP Contact:** John Gudas, (301) 975-3214, john.gudas@nist.gov

The long-term trend in microcircuits to get smaller, denser, and faster with each generation is approaching some serious roadblocks. One is the need for improved electrical insulating materials. The speed of a signal pulse in a conductor is partially a function of the properties of the insulator around it, in particular the insulator's dielectric constant — the lower the dielectric constant, the faster the pulse propagates. Increased switching speeds in microcircuits and denser packing of circuits both require conductor lines to be moved closer and closer together. But the conductors have to be far enough apart to avoid inducing signals in each other — so-called "cross-talk" — which also depends on how low the dielectric constant of the insulator can be pushed. Vacuum is the ideal insulator, and air is almost as good, but neither is particularly practical for commercial devices. For real applications, the designer wants a low-density material which is able to withstand the high processing temperatures associated with the manufacture of devices, and has a thermal expansion coefficient close to that of the substrate.

IBM has developed some organic polymers with carefully controlled structures that meet the needs for insulators in current-generation devices but are inadequate for the systems predicted to emerge in the next decade. For those devices, IBM is developing unique polymer insulating foams with dielectric constants below 2, and thermal and mechanical properties equivalent to the best current polymer insulators. The new foams will have closed-cell pores on a molecular scale. Three possible routes for producing these novel "nano-foams" are being pursued and evaluated. IBM is collaborating with the Virginia Polytechnic Institute, Exfluor Research, and Sandia National Laboratory in carrying out the research and, if successful, will transfer the technology to U.S. vendors.

**Start Date:** March 1993
**End Date:** February 1996

## *Materials*

### Ultra-low K Dielectric Materials for High Performance Interconnects

**Participants:** Texas Instruments Dallas, TX
**Industry Contact:** Sheree Fitzpatrick, (214) 995-2984
**ATP Contact:** Ronald Marquardt, (301) 975-5440, ronald.marquardt@nist.gov

Miniaturization of features has enabled steady improvements in circuit speed and functional integration of high-performance integrated circuits (ICs). But further progress is threatened by the limitations inherent in current interconnect technology. The problem is that, as feature size decreases beyond a certain point, the delay caused by the interconnects impedes IC performance.

To overcome this problem, Texas Instruments is seeking to integrate novel dielectric (electrically insulating) materials into on-chip interconnects, and to employ an innovative device structure in order to shorten the typical 10-year cycle for introducing new materials into semiconductor processing. The ATP project will demonstrate the integration of both amorphous Teflon® (a polymer) and silicon-dioxide-based xerogel (a low-density material) into a semiconductor process flow. By accelerating the development of new interconnect technology and the commercial use of new materials, the project could give U.S. industry leadership in the high-performance segment of the projected $200 billion worldwide semiconductor market by the year 2000.

**Start Date:** March 1995
**End Date:** February 1998

*Semiconductor Packaging*

## Flip Chip Monolithic Microwave Integrated Circuit Manufacturing

**Participants:** Hughes Aircraft Company Torrance, CA
**Industry Contact:** Ken Conklin, (310) 517-6536
**ATP Contact:** Thomas Leedy, (301) 975-2410, thomas.leedy@nist.gov

Wireless systems - particularly for personal data communications - may be the next big wave in consumer electronics. Already there are an estimated 7 to 9 million cellular telephone subscribers in the U.S., and industry analysts expect a similar explosion in wireless data systems based on pocket-sized personal computers by the end of the decade. Other rapidly developing wireless technologies include geographic tracking and information systems for vehicles, and "personal radar" collision-avoidance systems for cars and trucks. Compact, efficient, affordable microwave transmitters and receivers will be essential to these applications.

One of the most promising technologies is based on monolithic microwave integrated circuits (MMICs), which basically do for microwave circuits what the integrated circuit did for transistors and resistors: create dense, complex miniaturized devices. Current MMIC chips present severe manufacturing problems, which drive up costs. They are built on substrates of gallium arsenide (GaAs) and require complex processing on both sides of the chip. To improve heat conduction, the chips must be quite thin — approximately 100 microns — which makes them fragile and unsuitable for automated assembly. The larger MMIC chips required for tomorrow's advanced applications are even more fragile and difficult to work with.

Hughes, a leader in MMIC research, is working to solve these problems by adapting the "flip-chip" technology for silicon ICs to GaAs MMIC chips. On flip chips, the contacts used to connect the chip to a circuit board are put on the surface of the chip, along with all the circuit elements. The contacts are raised slightly higher than the rest of the chip features, and the chip is flipped upside down to fasten to the circuit board (hence the name). MMIC flip chips, in principle, will be much cheaper to make, cheaper to use, and more reliable.

Flip-chip mounting is not new, at least to the silicon industry, but flip-chip processing for GaAs ICs is just beginning to emerge from the laboratory, and much research and development still needs to be done. High risk areas include: the mechanical integrity of unsupported air bridge interconnections; unsubstantiated design rules and circuit modeling elements for flip chip processing; a demonstration of the yield of the new process; and establishing the reliability of units made using the process.

**Start Date:** January 1994
**End Date:** December 1995

*Electronic Interconnection*

## Printed Wiring Board Interconnect Systems

**Participants:** National Center for Manufacturing Sciences (NCMS), Ann Arbor, MI

**Industry Contact:** Edward Miller, (313) 995-0300

**ATP Contact:** Thomas Leedy, (301) 975-2410, thomas.leedy@nist.gov

Printed wiring boards (PWBs) are often overlooked in discussions of microchips and other advanced electronic components, but they form the backbone of virtually every electronic product, providing connections between individual electronic devices. Although to date PWB technology has kept pace with the increased speed and complexity of microelectronics, it is approaching fundamental limits in materials and processes that must be overcome if the U.S. industry is to maintain a competitive position. (The U.S. share of the $25 billion world market dropped from 42 to 29 percent in 3 years.)

Members of the NCMS consortium, including AT&T, Texas Instruments, the Digital Equipment Corporation, and Hamilton Standard Interconnect, Inc., are working with the Sandia National Laboratories (U.S. Dept. of Energy) to develop a more consistent epoxy glass material with improved mechanical characteristics for PWBs, improved processes and process-control techniques to produce more reliable solder connections, improved methods and technologies for fine-line imaging on the boards, and a better technical understanding of the chemistry underlying key copper-plating processes. Nine hundred U.S. firms in the PWB industry could benefit.

**Start Date:** April 1991
**End Date:** April 1996

*Electronic Interconnection*

## Scalable High-Density Electronics based on Multifilm Modules

**Participants:** The American Scaled-Electronics Consortium, Taunton, MA

**Industry Contact:** Dr. Jack P. Salerno, (508) 824-6696

**ATP Contact:** Thomas Leedy, (301) 975-2410, thomas.leedy@nist.gov

A constant challenge in the electronics industry is to pack more semiconductor devices into smaller spaces. Miniaturization enhances the value and allows lighter, more powerful products - laptop computers, for example. However, attempts to increase greatly the scale of circuit fabrication have been accompanied by unacceptable defect levels. When a single integrated circuit fills an entire wafer, yields become far too low to be commercially acceptable. A possible alternate approach is to continue to make smaller-scale devices, where quality control is easier and yields are acceptably high, but to pack the completed circuits closer together.

Kopin Corporation, the coordinator of The American Scaled-Electronics Consortium (TASC), has developed the technology to fabricate thin-film circuits on single-crystal silicon substrates, and then detach the circuit from the substrate in a film only a few microns thick which can then be transferred to an alternate substrate. TASC goal is to extend this technology to complex, multicircuit modules. Multiple thin-film circuits could be laminated on a glass substrate, for example, as part of a compact display device. Even more challenging, several thin-film circuits could be stacked atop each other to form extremely dense, three-dimensional circuit packages. To achieve this, the thin-film circuit technology must be meshed with methods to position components with micron-scale alignment, a suitable technology devised for connecting the individual circuits, and an adhesive developed to bond the devices together. All of these have been studied by the Microelectronics and Computer Technology Corporation (MCC) and their member companies, which make up the balance of TASC. A test of the multi-film module technology was to fabricate a large-area active matrix flat-panel display with on-board drivers and logic on a glass-based substrate.

**Start Date:** September 1992
**End Date:** September 1995

*Assembly*

## A Product-Family-Based Framework for Computer Integrated Manufacturing

**Participants:** IBM Corporation Charlotte, NC
**Industry Contact:** Sue Parliament, (407) 443-8753
**ATP Contact:** Barbara Goldstein, (301) 975-2304,
barbara.goldstein@nist.gov

In the nearly trillion dollar electronics industry, speed and agility often determine success in a marketplace that renders new products obsolete within months. Computer-integrated manufacturing is key to responding quickly to market opportunities and competitive challenges. But with an estimated 85 percent of installed CIM software developed in-house, upgrades and other system changes are an onerous task. Much of the bottleneck is at the production end, where specific applications often are isolated from other processes or are linked by specially written computer codes. As a consequence, changing an application's software requires costly, time-consuming reprogramming efforts. Eliminating incompatibilities in manufacturing and business software could trim production lead times by 40 to 60 percent.

IBM is tackling this problem with a bottom-up approach by creating an automation tool suite, enabling commercial software vendors to rapidly develop, maintain, and join families of interoperating products—sets of manufacturing and business applications that work together and can be updated in parallel. With collaborators from the University of North Carolina in Charlotte, and in consultation with its customers and software suppliers, IBM is working to devise a reference model to guide development of interoperable products, made by individual vendors or by alliances of software suppliers that establish their own voluntary standard within the framework so that they can provide families of products targeted to specific processes or types of manufacturers.

IBM's tool suite includes, for example, "re-engineering assistants" for updating and linking pre-existing "legacy" software and a "workbench" for specifying and documenting how products interoperate and for maintaining that interoperability over successive generations of products. The highly automated tools should reduce much of the manual programming labor now required to create interacting applications, thereby lowering cost barriers that deter commercial vendors from developing software for the factory floor. At the end of the project, IBM will demonstrate a prototype family of manufacturing applications for assembling and testing electronic cards.

**Start Date:** February 1995
**End Date:** November 1996

*Assembly*

## Solder Jet Technology Development

**Participants:** MicroFab Technologies, Inc. Plano, TX
**Industry Contact:** David B. Wallace, (214) 578-8076
**ATP Contact:** Gerald Ceasar, (301) 975-5069, gerald.ceasar@nist.gov

Trends in consumer electronics towards smaller size, lighter weight, and greater power and complexity all are straining today's electronic packaging technologies. In response, manufacturers have developed a variety of innovative packaging systems that pack greater and greater functionality and components in less and less space. But these high-density components require equally high-density methods for soldering the leads to circuit board contacts. At present, the solutions involve complex, expensive, and time-consuming processes including photolithography and (for very demanding situations) vapor deposition, etching, or plating.

MicroFab Technologies is pursuing an elegant alternative — "write" the solder patterns on circuit boards with the high-temperature equivalent of an ink-jet printer. MicroFab specializes in unusual applications of ink-jet technology, and their preliminary research suggests that the basic concept could be applied to deliver fine molten drops of solder to circuit boards rapidly and with precise control. The proposed "solder jet" would be far more flexible than any existing soldering system - probably driven directly from CAD images of the solder pattern - thus greatly reducing prototype and development time. It would also allow manufacturing techniques that are impossible or unfeasible with current technology, such as localized replacement of solder on boards (for rework or custom connections), depositing solder in different thicknesses on the same board (components differ in the amount of solder required for the best connection), or using more than one type of solder on the same board (temperature-sensitive components could be attached with lower-temperature solder after other components already are in place.)

Project objectives include the development of "solder jet" dispensers for both low- and high-temperature solders capable of producing 50 micrometer droplets on demand at rates up to 4,000 per second, and prototype electronic assembly equipment using the dispensers.

**Start Date:** January 1994
**End Date:** December 1996

# *APPENDIX I: ABBREVIATIONS*

| | |
|---|---|
| AMP | Advanced Materials Program |
| ANA | automatic network analyzer |
| AP | application protocol |
| ATP | Advanced Technology Program |
| BKD | backscatter Kikuchi diffraction |
| CAD | computer aided design |
| CIM | computer integrated manufacturing |
| CIMF | computer integrated manufacturing framework |
| CTE | coefficient of thermal expansion |
| DC | direct current |
| FTIR | Fourier transform infra-red |
| GaAs | gallium arsinide |
| IEEE | Institute of Electrical and Electronics Engineers |
| IGES | Initial Graphics Exchange Specification |
| IPC | Institute for Interconnecting and Packaging Electronic Circuits |
| ISHM | International Society for Hybrid Microelectronics |
| ITRI | Interconnection Technology Research Institute |
| LCR | inductance, capacitance, resistance |
| LEP | layered electrical product |
| MCC | Microelectronics and Computer Technology Corporation |
| MCM | multi-chip module |
| MMACE | microwave and millimeter-wave advance computational environment |
| MMIC | monolithic microwave integrated circuits |
| NBS | National Bureau of Standards |
| NCMS | National Center for Manufacturing Sciences |
| NIST | National Institute of Standards and Technology |
| NMR | nuclear magnetic resonance |
| NSMP | National Semiconductor Metrology Program |
| OIDA | Optoelectronics Industry Development Association |
| PCA | printed circuit assembly |
| PCB | printed circuit board |
| PWB | printed wiring board |
| RF | radio frequency |
| SEM | scanning electron microscope |
| SEMATECH | Semiconductor MANUFACTURING TECHnology |
| SEMI | Semiconductor Equipment and Materials International |
| Si | Silicon |
| SIA | Semiconductor Industry Association |
| SRC | Semiconductor Research Corporation |
| STEP | Standard for the Exchange of Product Model Data |
| TASC | The American Scaled-Electronics Consortium |
| TMA | thermal mechanical analyzer |
| U.S. | United States |
| WWW | World Wide Web |

# *APPENDIX II: COLLABORATIONS*

## Industry

AMP
Allied Signal Laminate Systems
Analogy
ArlonCorp.
AT&T Bell Laboratories
AT&T/Richmond
Cascade Microtech, Inc.
DELCO Electronics
Dielectric Labs
Digital Equipment Corporation
Dow Chemical Co.
ECI Technologies
Eastman Kodak
Edison Welding Inst.
Ford Microelectronics Inc,
Ford Motor Company
General Electric Company
General Photonics Corp.
Hamilton Standard International/UTRC
Harris Semiconductor
Hughes Microelectronics
Hughes Aircraft Company
IBM/Endicott
MicroFab Technologies, Inc.
Motorola
National Semiconductor Corp.
Plaskon, Inc.
Rockwell International
Rockwell Science Center
Rogers Corporation
TRW Inc.
Taconic Plastics
Tektronix, Inc.
Texas Instruments/Austin
Texas Instruments/Dallas
Trans-Tech
Universal Instruments

## Academia

Cornell University
Georgia Institute Of Technology
Lehigh University
Loughborough University of Technology
Marquette University
Purdue University
Rensselaer Polytechnic
State University of New York at Binghamton
Tel Aviv University, Tel Aviv, Israel
University of Arizona
University of Colorado
University of Delaware
University of Greenwich
University of Maryland
University of Massachusetts
University of Texas at Austin
University of Wisconsin

## Government Agencies

National Aeronautics and Space Administration-
Jet Propulsion Lab
Naval Surface Warfare Center - Crane Division
U.S. Department of Energy, Sandia National
Laboratories
U.S. Air Force, Newark Air Force Base
U.S. Air Force, Rome Laboratories

## Consortia, Standards Bodies, Associations, Other

EIA/JEDEC Committee JC-15
IPC
IPC Steam Aging Task Group
ISHM
ITRI
MCC
NCMS
SEMATECH
SEMI
SEMI/SEMATECH
SRC

# *APPENDIX III: PUBLICATIONS*

## Strategies and Activities

Michael A. Schen, ed., *Metrology and Data for Microelectronic Packaging and Interconnection*, Results of a joint workshop, May 5-6, 1994, NISTIR 5520, November 1994.

J.A. Carpenter, Jr., *Measurements of Properties of Materials in Electronic Packaging*, in Materials for Electronic Packaging, D. Chung ed., Butterworth-Heinemann, 80 Montvale Avenue, Stoneham, MA 02180. 341-360, 1995.

M. Schen, R. Scace, T. Leedy, *NIST Strategies, Activities and Collaborations in Electronics Packaging, Interconnection and Assembly*, Proceedings of the Eleventh Biennial University Government Industry Symposium, IEEE Special Publication 95CH35779, Austin, TX, pgs. 77-83, 1995.

M.A. Schen, G.T. Davis, F.I. Mopsik, W.L. Wu, W.E. Wallace, J.R. Manning, C.A. Handwerker, D.T. Read, *Electronics Packaging Materials Research at NIST*, in Electronic Packaging Materials Science VIII, R.C. Sundahl, K.A. Jackson, K-N. Tu, P. Børgesen, ed., Proceedings of the Materials Research Society (Materials Research Society, Pittsburgh, PA) 390, pgs. 19-32, 1995.

## Adhesion of Polymers: X-ray and Neutron Reflectivity Techniques

W. Wu, W.J. Orts, J. H. van Zanten, B.M. Fanconi, *Density Profile of Spin Cast Polymethylmethacrylate Thin Films*, J. Polym. Sci. Part B: Polymer Physics, 32, 2475, 1994.

W. Wu, *Off-specular Reflection from Flat Interfaces*, J. Chem. Phys., 101(5), 4198, 1994.

W. Wu, J. H. van Zanten and W. J. Orts, *Glass Transition Temperature of Ultrathin Polymer Films On Silicon*, Intl. Soc. Hybrid Microelec. , THP1-2, Boston, Nov., 1994.

W. Wu, M. Kent, *Moisture Adsorption at Polymer/Silicon Wafer Interface*, Mat. Res. Soc. Symp. Proc., 338, 565-569, 1994.

W. Wu, J.H. Van Zanten, W.J. Orts, *Thermal Expansion Measurements of Thin PMMA Films*, Macromolecules, 28, 771, 1995.

W. Wu, W.J. Orts, C.J. Majkrzak, D.L. Hunston, *Water Adsorption at Polyimide/Silicon Water Interface*, Polymer Engineering and Science, 35(12), 1000-1004, 1995.

W. Wu, W.E. Wallace, J. van Zanten, *Glass Transition Temperature of Ultrathin Polymer Films on Silicon*, in Low-Dielectric Constant Materials - Synthesis and Applications in Microelectronics, T-M. Lu, S.P. Murarka, T.S. Kuan, C.H. Ting eds., Proceedings of the Materials Research Society, (Materials Research Society, Pittsburgh, PA) 381, 147-152, 1995.

W.E. Wallace, W. Wu, , *A Novel Method for Determining Thin Film Density by Energy-Dispersive X-ray Reflectivity*, App. Phys. Lett., 67, 1203-1205, 1995.

W.E. Wallace, J.H. van Zanten, W. Wu, *Influence of an Impenetrable Interface on a Polymer Glass-Transition Temperature*, Physical Review E, 52(4), R3329-R3332, 1995.

P. Chin, W. Wu, *Determination of Oxygen Number Density Profiles in Chromium and Aluminum Films by X-ray and Neutron Reflectivity*, to be submitted.

## Mechanics of Thin Interlayers: Viscoelastic and Fracture Behaviors

M.Y. M. Chiang, H. Chai, *Plastic Deformation Analysis of Fracture in Constrained Interlayers Subjected to Shear Loading*, Proc. Am. Soc. Comp., 9th Tech. Conf., 629-639, 1994.

M.Y.M. Chiang, *Modified Mohr-Coulomb Plasticity Model for Nonlinear Fracture Analysis of Polymeric Interlayer*, Proceedings ANTEC, '95, Society of Plastics Engineers, May 1995.

H. Chai, M.Y.M. Chiang, *Plastic Deformation Analysis of Cracked Adhesive Bonds Loaded in Shear*, Int. J. Solids Structures, **31**(18), 2477-2490, 1994.

M.Y.M. Chiang, G.B. McKenna, J. Yuan, *A Viscoelastic Micro-Mechanical Analysis for Dimensional Stability of a Composite Layer*, Polymer Engineering and Science, **34**(24), 1815-1822, 1994.

H. Chai, M.Y.M. Chiang, *A Crack propagation Criterion Based on Local Shear Strain in Adhesive Bonds Subjected to Shear*, submitted, Journal of Mechanics, Physics of Solids.

## Moisture Effects in Electronic Packaging Resins

R.J. Schadt and D.L. VanderHart, *Solid-State Proton NMR of a Glassy Epoxy Exposed to Water,* Macromolecules 28, 3416, 1995.

## Polymer Cure and Performance

Brian Dickens, *Monitoring the Cure of Thin-Layer Polyimides on Glass Substrates with Photoacoustic Infrared Spectroscopy*, ISHM '94 Proceedings, 501, 1994.

Aimé S. DeReggi, Siegfried Bauer, *Adaptation of the Thermal Pulse Method to the Measurement of the Thermal Diffusivity of Dielectric Films on Conducting Substrates*, in Proceedings of the Conference on Electrical Insulation and Dielectric Phenomenon, October 1995, in press.

## Dielectric Measurements of Materials: DC to 1 GHz

F.I. Mopsik, *Precision Time-domain Dielectric Spectrometer*, Rev. Sci. Instrum., **55**, 79, 1984.

F.I. Mopsik, *The Transformation of Time-domain Relaxation Data into the Frequency Domain*, IEEE Trans. Elec. Insul., **EI-20**, 957, 1985.

F.I. Mopsik, *Two-Fluid Measurements on Thin Films*, NIST Technical Note, **1294** (United States Department of Commerce, Gaithersburg, MD), May 1992.

## Dimensional Stability of Polymers

M.A. Schen, G.T. Davis, F. Mopsik, W. Guthrie, W.T. Chen, E. Livingston, L. Lee, W. Robbins, C. Lee, P. Henderson, M. Li, M. Pecht, C.Y. Lee, J. Dion, P.S. Ho, H. Li, J. Kelly, *An Industry / Government / University Partnership: Measuring Sub-Micrometer Strain in Polymer Films*, Proc. of the 1994 IPC Technical Conference (Institute for Interconnecting and Packaging Electronic Circuits, Lincolnwood, IL) April 24-27, P4.3.1-P4.3.7, 1994.

## Electromagnetic Properties of Materials

J. Baker-Jarvis, M.D. Janezic, *Open-ended Coaxial Probes for Nondestructive Testing of Substrates and Circuit Boards*, in Microwave Processing of Materials IV, Proceedings of the Materials Research Society (Materials Research Society, Pittsburgh, PA) **347**, 215-220, 1994.

C.A. Jones, *Overview of Substrate/Thin Film Measurement Techniques*, Proceedings of the 1994 Wireless Circuits, Interconnection & Assembly Workshop, Scottsdale, AZ, 16-19 October 1994.

C.M. Weil, *The NIST Metrology Program on Electromagnetic Characterization of Materials*, in Materials and Processes for Wireless Communications, Ceramic Trans. (Amer. Ceramic Soc., Westerville, OH), **53**, 35-48, 1994.

## Electron Beam Moiré

James W. Dally, David T. Read, *Electron Beam Moiré*, Experimental Mechanics 33, 270-277, 1993.

David T. Read, James W. Dally, *Electron Beam Moiré Study of a GFRP Composite*, Transactions of the ASME--Journal of Applied Mechanics **61**, 402-409, 1994.

David T. Read, James W. Dally, *Local Strain Measurement by Electron Beam Moiré*, in Advances in Electronic Packaging 1993, Vol. 1, Proceedings of the ASME International Electronics Packaging Conference, Binghamton, New York, Sept. 29-Oct. 2, 1993, edited by Peter Engel and William Chen, EEP-Vol. 4-1, American Society of Mechanical Engineers, 163-169, 1993.

David T. Read, Elizabeth S. Drexler, *Local Deformation of Plated Through Holes Under Thermomechanical Loading*, in Mechanics and Materials for Electronic Packaging: Volume 2, Thermal and Mechanical Behavior and Modeling, Proceedings of the 1994 International Mechanical Engineering Congress and Exposition, November 6-11, 1994, edited by Michael Schen, Hiroyuki Abé, AMD-Vol. 187, American Society of Mechanical Engineers, 185-194, 1994.

D. T. Read, E. S. Drexler, I. Grosse, J. Benoit, J. DiTomasso, E. Bernard, D. Holzhauer, P. Rocci, M. Stoklosa, *Thermomechanical Behavior of a High Density Polymer Overlay MCM Interconnect Structure: Experiments and Analysis*, in Application of Fracture Mechanics in Electronic Packaging and Materials, Proceedings of the Symposium on Application of Fracture Mechanics in Electronic Packaging and Materials, American Society of Mechanical Engineers 1995 International Conference and Exposition, Nov. 12-17, in press, 1995.

David T. Read, James W. Dally, *Theory of Electron Beam Moiré*, Journal of Research of the National Institute of Standards and Technology, in press, 1996.

## Micromechanical Measurements

David T. Read, *A Microfabrication Approach to Mechanical Testing of Thin Films*, in Electronic Packaging Materials Science, Materials Research Society Symposium Proceedings, edited by E.D. Lillie, Paul Ho, R.J. Jaccodine, and Kenneth Jackson, **203**, 147-151, 1991.

Moti Szanto, David T. Read, *J-Integral Applied to Stress-Strain Concentrations*, Engineering Fracture Mechanics **43**, 401-415, 1992.

David T. Read, *In Situ Measurements of Strength and Ductility of Thin Films*, in Advances in Electronic Packaging 1992, Vol. 1, Proceedings of the First Joint ASME/JSME Conference on Electronic Packaging, April 9-12, 1992, edited by William Chen and Hiroyuki Abé, EEP-Vol. 1-1, American Society of Mechanical Engineers, 463-468, 1992.

David T. Read, James W. Dally, Moti Szanto, *Scanning Moire at High Magnification Using Optical Methods*, Experimental Mechanics **33**, 110-116, 1993.

Moti Szanto, James W. Dally, David T. Read, *A Hybrid Grid-Moiré Method for Measuring Strain and Displacement*, Optical Engineering **32**, 1043-1052, 1993.

David T. Read, James W. Dally, *Strength, Ductility and Fatigue Life of Aluminum Thin Films*, International Journal of Microcircuits and Electronic Packaging **16**, Number 4, 313-318, 1993.

David T. Read, James W. Dally, *A New Method for Measuring the Strength and Ductility of Thin Films*, Journal of Materials Research **8**, 1542-1549, 1993.

David T. Read, James W. Dally, *Mechanical Behavior of Aluminum and Copper Thin Films*, in Mechanics and Materials for Electronic Packaging: Volume 2, Thermal and Mechanical Behavior and Modeling, Proceedings of the 1994 International Mechanical Engineering Congress and Exposition, Chicago, Illinois, November 6-11, 1994, edited by Michael Schen, Hiroyuki Abé, AMD-Vol. 187, American Society of Mechanical Engineers, 41-49, 1994.

Robert R. Keller, John M. Phelps, David T. Read, *Tensile Deformation-induced Microstructures in Free-standing Copper Thin Films*, in Materials Reliability in Microelectronics IV, Proceedings of the Materials Research Society (Materials Research Society, Pittsburgh) **338**, 227-232, 1994.

David T. Read, James W. Dally, *Fatigue of Aluminum Thin Film Under Cyclic Axial Stress*, Journal of Electronic Packaging **117**, 1-6, 1995.

Shawn J. Cunningham, Wan Suwito, David T. Read, *Tensile Testing of Epitaxial Silicon Films*, in Transducers '95, Proceedings of The 8th International Conference on Solid-State Sensors and Actuators and Eurosensors IX, June 1995, **2**, 96-99, 1995.

## Stress Voiding and Electromigration Damage in Thin Metal Films

R. R. Keller, J. M. Phelps, D. T. Read, *Tensile Deformation-Induced Microstructures in Free-Standing Copper Thin Films*, in Materials Reliability in Microelectronics IV, Proceedings of the Materials Research Society, editors P. Borgesen, J. Sanchez, Jr., K. Rodbell, J. Coburn, W. Filter (Materials Research Society, Pittsburgh, PA) **338**, 227-232, 1994.

R. R. Keller, J. M. Phelps, D. T. Read, *Tensile and Fracture Behavior of Free-Standing Copper Films*, Materials

Science and Engineering A, submitted (1995).

## Lead-free Solders

U. R. Kattner, W. J. Boettinger, *On the Sn-Bi-Ag Ternary Phase Diagram*, Journal of Electronic Materials, 23, 601-608, 1994.

## Solderability Measurements and Optimization

W.J. Boettinger, C.A. Handwerker, L.C. Smith, *On the Wetting of the Intermetallics $Cu_6Sn_5$ and $Cu_3Sn$ by Pb-Sn Alloys*, in The Metal Science of Joining, M.J. Cieslak, J.H. Perepezko, S. Kang and M.E. Glicksman, eds., (TMS-AIME, Warrendale, PA.) p. 183-190, 1992.

R.J. Schaefer, F. S. Biancaniello, R.D. Jiggetts, *Preparation of Bulk Samples of Copper-Tin Intermetallics*, in The Metal Science of Joining, M.J. Cieslak, J.H. Perepezko, S. Kang and M.E. Glicksman, eds., (TMS-AIME, Warrendale, PA.) p. 175-181, 1992.

R.J. Fields, S.R. Low III, G.K. Lucey, *Physical and Mechanical Properties of Intermetallic Compounds Found in Solder Joints*, in The Metal Science of Joining, M.J. Cieslak, J.H. Perepezko, S. Kang and M.E. Glicksman, eds., (TMS-AIME, Warrendale, PA.) p. 165-174, 1992.

H.P.R. Frederikse, R.J. Fields, A. Feldman, *Thermal and Electrical Properties of Copper-Tin Intermetallics*, Journal of Applied Physics 72, p. 2879-2882, 1992.

W. J. Boettinger, C. A. Handwerker, U. R. Kattner, *Reactive Wetting and Intermetallic Formation*, in The Mechanics of Solder Alloy Wetting and Spreading, ed. D. Frear, F. M. Hosking, F. Yost (VanNostrand Reinhold, New York) 103-140, 1993.

J. A. Carpenter, Jr., B. Dickens, K. G. Kreider, J. R. Manning, R. L. Mattis, G. J. Piermarini, D. T. Read, and R. D. Evans, *NIST/NCMS Program on Electronic Packaging: First Update*, in Materials in Microelectronic and Optoelectronic Packaging, ed. H.C. Ling, K. Niwa, N. N. Shukla (American Ceramic Society, Westerville, Ohio) Ceramic Transactions, 33, 345-358 1993.

U. Bertocci, C. A. Handwerker, S. M. Hues, and W. J. Boettinger, *Oxidation of Cu-Sn and Ni-Sn Intermetallic Compounds*, in Proceedings of the Second International Symposium on the Corrosion and Reliability of Electronic Materials and Devices, ed. R. B. Comizzoli, J. D. Sinclair (The Electrochemical Society, Pennington, NJ) 99-118, 1993.

M. A. Schen, G. T. Davis, F. I. Mopsik, W. L. Wu, W. E. Wallace, J. R. Manning, C. A. Handwerker, D. T. Read, *Electronics Packaging Materials Research at NIST*, in Electronic Packaging Materials Science VIII, R. C. Sundahl, K. A. Jackson, K-N. Tu, P. Borgesen, ed., Proceeding of the Materials Research Society 390, pgs. 19-32, 1995.

R. J. Braun, B. T. Murray, W. J. Boettinger, G. B. McFadden, *Lubrication Theory for Reactive Spreading of a Thin Drop*, Phys. Fluids 7, 1797-1810, 1995.

## Metrology for Devices and Packages

A. R. Hefner and D. L. Blackburn, *Thermal Component Models for Electro-Thermal Network Simulation*, IEEE Transactions on Components, Packaging, and Microelectronic Technology Part A, pp.413-424, Sept. 1994.

J. Albers, *An Exact Recursion Relation Solution for the Steady-State Surface Temperature of a General Multilayer Structure*, IEEE Transactions on Components, Packaging, and Microelectronic Technology Part A, 31-38, March 1995.

D.L.Blackburn, *Natural Convection from an Array of Packages Mounted on a Horizontal Board in a Narrow Aspect Ratio Enclosure*, Thirteenth National Heat and Mass Transfer Conference, Surathkal, India, December 28-30, 1995, to be published.

## Electrical Characterization of Printed Wiring Board Interconnects

W.L. Gans, J.R. Andrews, *Time Domain Automatic Network Analyzer for Measurement of RF and Microwave Components*, NBS Technical Note 672, U.S. Department of Commerce, 1975.

O.B. Laug, T.M. Souders, D.R. Flach, *A Custom Integrated Circuit Comparator for High Performance Sampling Applications*, IEEE Trans. Instrum. Meas., **41**, 850, 1993.

N.G. Paulter, R.B. Stafford, *Reducing the Effects of Record Truncation Discontinuities in Waveform Reconstructions*, IEEE Trans. Instrum. Meas., **42**, 695, 1993.

N.G. Paulter, *A Causal Regularizing Deconvolution Filter for Optimal Waveform Reconstruction*, IEEE Trans. Instrum. Meas., **43**, 740, 1994.

N.G. Paulter, *A Fast and Accurate Method for Measuring the Dielectric Constant of Printed Wiring Board Materials*, submitted.

## Evaluation of Wire Bonding Technology

G. G. Harman and C. A. Cannon, *The Microelectronic Wire Bond Pull Test How to Use It, How to Abuse It*, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, **CHMT-1**, 203-210, 1978.

G. G. Harman and K. A. Harmison, *The Assessment of Hybrid Package Glass Metal Seal Reliability Using Acoustic-Emission Measurement Techniques*, International Journal of Hybrid Microelectronics, **5**, 248-259, 1982.

G. G. Harman, *Acoustic-Emission-Monitored Tests, for TAB Inner Lead Bond Quality*, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, **CHMT-5**, 445-453, 1982.

G. G. Harman, *The Microelectronic Ball-Bond Shear Test - A Critical Review and Comprehensive Guide to Its Use*, International Journal of Hybrid Microelectronics, **6**, 127-141, 1983. (Also invited (modified) and pub. in Solid State Technology 27(5), 186-197, 1984.)

Harman, G. G., and Wilson, C. L., *Materials Problems Affecting Reliability and Yield of Wire Bonding in VLSI Devices*, Proc. MRS Symposium on Electronics Packaging, San Diego, CA, Apr. 24-29, 1989, **154**, 401-413, 1989.

Harman, G. G., *Reliability and Yield Problems of Wire Bonding in Microelectronics*, in The Application of Materials and Interface Science, International Society for Hybrid Microelectronics (ISHM) Monograph, 1989.

Harman, G.G., *Low-End Cost Driven Packaging: The Neglected Area of Packaging Research*, The Intl J. of Electronic Packaging, 13(3), iii-V, 1990.

Kopanski, J. J., Blackburn, D. L., Harman, G. G., Berning, D. W., *Assessment of Reliability Concerns for Wide-Temperature Operation of Semiconductor Devices and Circuits*, Proceedings of the First International High Temperature Electronics Conference, Albuquerque, New Mexico, June 16-20, 137-142, 1991.

Harman, G. G., *Wire Bonding--Towards 6σ Yield and Fine Pitch*, Proc. 1992 IEEE, 42nd Electronic Technology and Components Conference, May 18-20, 1992, 903-910. (Also Transactions on CHMT, 15, 1005-1012, Dec. 1992).

*Recommended Practice For the Bonding and Metallization Used in Radiation Detectors Prepared for use in GOES, TIROS, and Other Space Craft*, NIST Special Publication 400-94, 97-102, 1994.

Harman, G.G., *Wire Bonding to Multichip Modules and Other Soft Substrates*, in NATO ASI Series (Kluwer Academic Publishers), in press, 1995 or early 1996. (Earlier work on this subject under the same name was given in Proc. 1995 Intl Conf., on Multichip Modules, April 19-21, 1995, Denver CO, 292-301.)

Harman, G.G., *Metallurgical Interactions In High Temperature Electronics*, in High Temperature Electronics, IEEE Press, 1996, in press.

## High-Speed Electromagnetic Metrology

R. B. Marks, D. F. Williams, *Characteristic Impedance Determination using Propagation Constant Measurement*, IEEE Microwave and Guided Wave Letters 1, 141-143, 1991.

R. B. Marks, *A Multiline Method of Network Analyzer Calibration*, IEEE Transactions on Microwave Theory and Techniques, 39, 1205-1215, 1991.

D. F. Williams, R. B. Marks, *Transmission Line Capacitance Measurement*, IEEE Microwave and Guided Wave Letters, 1, 243-245, 1991.

D. F. Williams, R. B. Marks, *Comments on 'Characterization of Resistive Transmission Lines by Short-Pulse Propagation'*, IEEE Microwave and Guided Wave Letters 2, 346, 1992.

D. F. Williams, R. B. Marks, *Frequency-Dependent Transmission Line Parameters*, First IEEE Topical Meeting on Electrical Performance of Electronic Packaging, 125-127, Apr. 1992.

R. B. Marks, D. F. Williams, *Accurate Experimental Characterization of Interconnects: A Discussion of 'Experimental Electrical Characterization of Interconnects and Discontinuities in High-Speed Digital Systems'*, IEEE Transactions on Components, Hybrids, and Manufacturing Technology 15, 601-602, 1992.

R. B. Marks, D. F. Williams, *A General Waveguide Circuit Theory*, Journal of Research of the National Institute of Standards and Technology 97, 533-562, 1992.

D. F. Williams, R. B. Marks, *Calibrating On-Wafer Probes to the Probe Tips*, 40th ARFTG Conference Digest, 136-143, Dec. 1992.

R. B. Marks, D. F. Williams, *Interconnection Transmission Line Parameter Characterization*, 40th ARFTG Conference Digest, 88-95, Dec. 1992.

D. F. Williams, R. B. Marks, *Accurate Transmission Line Characterization*, IEEE Microwave and Guided Wave Letters, 3, 247-249, 1993.

D. F. Williams and R. B. Marks, *LRM Probe-Tip Calibrations with Imperfect Resistors and Lossy Lines*, 42nd ARFTG Conference Digest, 32-36, Dec. 1993.

R. B. Marks, D. F. Williams, *Verification of Commercial Probe-Tip Calibrations*, 42nd ARFTG Conference Digest, 37-44, Dec. 1993.

D. F. Williams, R. B. Marks, *On-Wafer Impedance Measurement on Lossy Substrates*, IEEE Microwave and Guided Wave Letters, 4, 175-176, 1994.

R. B. Marks, D. F. Williams, *Microwave Characterization of Printed Circuit Transmission Lines*, NEPCON East 1994 Proceedings, 520-527, June 1994.

D. C. DeGroot, J. A. Beall, R. B. Marks, D. A. Rudman, *Tunable Microwave Properties of $YBa_2Cu_3O_{7-\delta}/SrTiO_3$ Thin Film Transmission Lines*, Applied Superconductivity Conference, Oct. 1994.

L. A. Hayden, R. B. Marks, *Accuracy in Time Domain Transmission Line Measurements*, Third IEEE Topical Meeting on Electrical Performance of Electronic Packaging, Nov. 1994.

R. B. Marks, D. F. Williams, *Accurate Electrical Characterization of High-Speed Interconnections*, Proceedings of the International Symposium on Microelectronics, 96-101, Nov. 1994.

D. F. Williams, R. B. Marks, *Compensation for Substrate Permittivity in Probe-Tip Calibration*, 44th ARFTG Conference Digest, 20-30, Dec. 1994.

L. A. Hayden, R. B. Marks, J. B. Rettig, *Accuracy and Repeatability in Time Domain Network Analysis*, 44th ARFTG Conference Digest, 39-46, Dec. 1994.

R. B. Marks, L. A. Hayden, J. A. Jargon, F. Williams, *Time Domain Network Analysis using the Multiline TRL Calibration*, 44th ARFTG Conference Digest, 47-55, Dec. 1994.

D. F. Williams, R. B. Marks, *LRM Probe-Tip Calibrations using Nonideal Standards*, IEEE Transactions on Microwave Theory and Techniques, 43, 466-469, 1995.

R. B. Marks, D. F. Williams, *Comments on 'Conversions Between S, Z, Y, h, ABCD, and T Parameters which are Valid for Complex Source and Load Impedances'*, IEEE Transactions on Microwave Theory and Techniques, 43, 914-015, 1995.

R. B. Marks, J. A. Jargon, C. K. Pao, C. P. Wen, Y. C. Shih, *Microwave Characterization of Flip-Chip MMIC Interconnections*, 1995 IEEE MTT-S International Microwave Symposium Digest, 1463-1466, May 15-19, 1995.

R. B. Marks, J. A. Jargon, C. K. Pao, C. P. Wen, *Microwave Characterization of Flip-Chip MMIC Components*, 45th Electronic Components and Technology Conference Digest, 343-350, May 21-24, 1995.

D. C. DeGroot, J. A. Beall, R. B. Marks, D. A. Rudman, *Microwave Properties of Voltage-Tunable $YBa_2Cu_3O_{7-\delta}/SrTiO_3$ Coplanar Waveguide Transmission Lines, IEEE Transactions on Applied Superconductivity*, 5, 2272-2275, 1995.

R. B. Marks, D. F. Williams, *Electrical Characterization Methods for High-Speed Interconnections*, International Journal of Microcircuits and Electronic Packaging, 18, Third Quarter, 1995.

R. B. Marks, J. A. Jargon, C. K. Pao, C. P. Wen, *Electrical Measurements of Microwave Flip-Chip Interconnections*, Proceedings of the 1995 International Symposium on Microelectronics, 424-429, Oct. 1995.

R. B. Marks, D. C. DeGroot, J. A. Jargon, *High-Speed Interconnection Characterization using Time Domain Network Analysis*, Advancing Microelectronics, 22, 35-39, Nov.-Dec., 1995.

D. F. Williams, J.B. Schappacher, *Line-Reflect-Match Calibrations with Nonideal Microstrip Standards*, 46th ARFTG Conference Digest, Dec. 1995.

J. A. Jargon, R. B. Marks, *Two-Tier Multiline TRL for Calibration of Low-Cost Network Analyzers*, 46th ARFTG Conference Digest, 1-8, Dec. 1995.

D. C. DeGroot, R. B. Marks, *The Effects of Instrument Settings on Calibrated Time-Domain Network Analysis*, 46th ARFTG Conference Digest, 19-28, Dec. 1995.

## Automated Electronics Manufacturing

T. F. Leedy, *NIST Developing Neutral Format for HMA Manufacturers*, Navy Manufacturing Technology Program Report, Dept. of the Navy (Naval Industrial Resources Support Activity, Philadelphia, PA) pp. 4-5, Nov 1989.

C. Parks, R. McCollough, C. Azu, L. Savage, P. Toomey, T. Makoski, *Initial Graphics Exchange Specifications Hybrid Microcircuit Applications Protocol*, Nat. Inst. Stand. and Tech. (U.S.), NIST TN 1295, Jan 1993.

C. Parks, *Applying Hypertext to Managing Versions of a Standard*, Nat. Inst. Stand. and Tech. (U.S.), NISTIR 5245, Sept 1993.

C. Parks, R. Meagher, *Improving the Quality of Model Reviews with Computer Hypertext Technology*, in Proc. IDEF Users Group 1993 Fall Conference on Global Competitiveness--Integrating Process, Information and Technology, October 18-21, 1993, Salt Lake City, UT, pp. 28-38, 1993.

B. L. M. Goldstein, *Electronic Commerce for the Electronics Industry*, Proc. Conference for Electro International '94, Institute of Electrical and Electronics Engineers, May 10-12, 1994, Boston, MA, 1994.

C. Parks, *Demonstration: World Wide Web for Distribution of Users Group Information on Internet*, Proc. IDEF Users Group 1994 Spring Conference on Reinventing the Enterprise...Technologies of Change, May 23-26, 1994, Richmond, VA, pp. 4-6, May 1994.

M. J. McLay, *The Role of Standards in Vacuum Electronics*, Proc. Vacuum Electronics Annual Review, Department of Defense, June 29-July 1, 1993, Crystal City, VA, pp. II-29 to II-33, Jun 1994.

C. Parks, E. Reid, G.F. Morea, *Operating Procedures and Life Cycle Documentation for the Initial Graphics Exchange Specification*, Nat. Inst. Stand. and Tech. (U.S.), NISTIR 5666, June 1995.

James A. St. Pierre, S.L. Stewart, *Roadmap for the Computer Integrated Manufacturing Application Framework*, SEMATECH Technology Transfer Document 95052825A-ENG, June 1995.

James A. St. Pierre, S.L. Stewart, *Roadmap for the Computer Integrated Manufacturing Application Framework*, Nat. Inst. Stand. and Tech. (U.S.), NISTIR 5679, June 1995.

# *INDEX*


Adhesion, 5
Assembly
  Design Tools, 16
  Electronic Data Exchange, 23
  Interconnect Design, 16
  Intermetallics, 18
  Solder, 16
  Solder Jetting, 17
  Solderability and Wetting, 15, 18
CIM, 23, 29
CTE, 5, 10
Cure, 8
Data Exchange
  Product Exchange Standards, 23
  Standards, 23
Data Transfer Standards, 23
Design for Manufacture, 16
Dielectric Constant, Loss, 9, 11, 20
Dielectric Materials, 24, 25
Dimensional Stability, 10
Electrical Test, 11
  Frequency Domain Test, 19
  Frequency, Time Domain Test, 20, 22
  GHz Measurements, 22
  Polymers, 9
  PWB, 20
  Standards, 22
  Time Domain Reflectometry, 19
Electromigration, 14
Electron Beam Moiré, 12
Encapsulants, 7
Fatigue, 13
Fine Pitch Interconnection, 30
Finite Element Modeling, 6, 12, 13
Flip-chip, 26
Fracture Mechanics, 6
Frequency Domain Test, 9, 11, 19, 20, 22
GaAs, 26
GHz Measurements, 11, 22
Glass Transition Temperature, 5
High Density Interconnects, 27, 28
IGES, 23
Infrared Spectroscopy, 8
Integrated Tool Suite, 29
Interconnect Design, 16
Interconnects
  CTE, 10
  Dielectric Constant, Loss, 9
  Dimensional Stability, 10
  Electrical Test, 9, 11, 20, 22
  Electromigration, 14
  Electron Beam Moiré, 12
  Fatigue, 13
  Frequency Domain Test, 9, 11
  GHz Measurements, 11
  MMIC, 22
  PWB, 20
  RF/Microwave Test, 11
  Standards, 22
  Stress Voiding, 14
  Stress, Strain Testing, 13
  Thin Film Mechanics, 12, 13
  Time Domain Test, 9
  Wire Bonding, 21
Interfaces, 5, 7
Intermetallics, 18
Lead-free Solders, 15
Materials
  Low Dielectric Constant, 24, 25
  PWB, 27
Materials Metrology
  Adhesion, 5
  CTE, 5, 10
  Dielectric Constant, Loss, 9, 11
  Dimensional Stability, 10
  Electrical Test, 9, 11
  Electromigration, 14
  Encapsulants, 7
  Fatigue, 13
  Finite Element Modeling, 6, 12, 13
  Fracture Mechanics, 6
  Frequency Domain Test, 9, 11
  GHz Measurements, 11
  Glass Transition Temperature, 5
  In Situ Strain, 12
  Interconnect Design, 16
  Interconnects, 18
  Interfaces, 5, 7
  Lead-free Solders, 15
  Mechanical Properties, 6, 12, 13
  Metals, 12, 13
  Modeling, 6, 15
  Moisture, 5, 7, 8
  NMR, 7
  Photoacoustic Spectroscopy, 8
  Polymer Cure, 8
  Polymer Strain, 10
  Popcorning, 7, 8

RF/Microwave Test, 11
Shear Deformation, 6
Solder, 15-18
Solder Jetting, 17
Solderability and Wetting, 15, 18
Stress, 8
Stress Voiding, 14
Stress, Strain Testing, 13
Thermal Conductivity, 8
Thin Film Mechanics, 6, 12, 13
Time Domain Test, 9
Mechanical Properties
Fatigue, 13
Finite Element Modeling, 6, 12, 13
Shear Deformation, 6
Stress, Strain Testing, 13
Metals
Fatigue, 13
Stress, Strain Testing, 13
Micro-tensile Testing, 13
MMIC, 11, 22, 26
Modeling
Electrical Test, 19
Solderability and Wetting, 15, 18
Thermal Measurements, 19
Thin Film Mechanics, 6, 12, 13
Moire Interferometry, 12
Moisture, 5, 7, 8
Multichip Modules, 28
Wire Bonding, 21
Nano-foams, 24
Neutron Reflectivity, 5
NMR, 7
On-chip Interconnects
Low Dielectric Constant Materials, 24, 25
Package-, Assembly-level Metrology
Dielectric Constant, Loss, 20
Electrical Test, 19, 20, 22
Frequency Domain Test, 20
GHz Measurements, 22
Interconnects, 20, 21
MMIC, 22
Modeling, 19
PWB, 20
Standards, 22
Thermal Measurements, 19
Time Domain Test, 20
Wire Bonding, 21
Photoacoustic Spectroscopy, 8
Polymer
Adhesion, 5
CTE, 5, 10
Cure, 8
Electrical Test, 9
Encapsulants, 7
Finite Element Modeling, 6
Fracture Mechanics, 6
Glass Transition Temperature, 5
Infrared Spectroscopy, 8
Interfaces, 5, 7
Mechanical Properties, 6
Moisture, 5, 7, 8
NMR, 7
Photoacoustic Spectroscopy, 8
Popcorning, 7, 8
Shear Deformation, 6
Stress, 8
Thermal Conductivity, 8
Thin Film Mechanics, 6
Polymer Cure, 8
Popcorning, 7, 8
Product Exchange Standards, 23
PWB
Dimensional Stability, 10
Electrical Test, 11, 20
Electronic Data Exchange, 23
High Density Interconnects, 27
Thin Film Mechanics, 6
Residual Stress, 8
RF/Microwave Test, 11, 22
Semiconductor Packaging
Adhesion, 5
CTE, 5
Electrical Test, 19
Electronic Data Exchange, 23
Encapsulants, 7
Finite Element Modeling, 6
Fracture Mechanics, 6
Interfaces, 5, 7
Mechanical Properties, 6
Modeling, 19
Moisture, 5, 7, 8
Photoacoustic Spectroscopy, 8
Polymer Cure, 8
Popcorning, 7, 8
Shear Deformation, 6
Stress, 8
Thermal Conductivity, 8
Thermal Measurements, 19
Thin Film Mechanics, 6
Shear Deformation, 6
Software, 16
Solder
Design Tools, 16
Intermetallics, 18
Jetting, 17, 30

Joint Geometry, 16
Joint Performance, 17
Solderability and Wetting, 15, 18
Steam Aging Test, 18
Solder Jetting, 17, 30
Solder Wetting, 15, 18
Solderability, 15, 18
Standards, 22
Steam Aging Test, 18
STEP, 23
Stress Voiding, 14
Stress, Strain Testing, 13
Thermal Conductivity, 8
Thermal Tests, 19
Thin Film Mechanics, 6, 12, 13
Thin Film Technology, 28
Time Domain Test, 9, 19, 20, 22
TMA, 10
Wetting Balance Test, 18
Wire Bonding, 21
X-ray Reflectivity, 5

Additional paper copies of this report may be obtained by contacting:

**National Institute of Standards and Technology (NIST)**
Michael A. Schen
Blg 224, Room B320, Gaithersburg, MD 20899
tel. (301) 975-6741; FAX (301) 869-3239
michael.schen@nist.gov

or

**National Technical Information Service (NTIS)**
5285 Port Royal Road, Springfield, VA 22161
tel. (703) 487-4650
http://www.fedworld.gov/ntis/ntishome.html

This document may also be obtained after July 1996 through the World Wide Web at the following Internet addresses.

**National Institute of Standards and Technology (NIST)**
Materials Science and Engineering Laboratory
http://www.msel.nist.gov

and

Electronics Packaging, Interconnection and Assembly Materials Program
http://www.msel.nist.gov/~interconnects